Steady-state thermal mapping of electronic devices and circuits with multi-layer stack assembly by analytical relationships

M.Montesi[1], P.E.Bagnoli[1*], C.Casarosa[2], G.Pasquinelli[3]

[1]*Dept. of Information Engineering, University of Pisa, Via Diotisalvi 2, I-56100 Pisa, Italy,*
email : p.bagnoli@iet.unipi.it
[2]*Dept. of Energetics, University of Pisa, Via Diotisalvi 2, Pisa, Italy*
[3]*Lab. Materials and Structures Mechanics I.S.T.I. "A. Faedo",C.N.R., via G. Moruzzi, I-56100 Pisa, Italy*

Abstract

This paper deals with an analytical model for the steady-state temperature mapping of electronic devices and system boards. It is devoted to solid structures which can be schematically modelled as a stack of several homogeneous layers of different materials and different sizes, also with various degree of asymmetry, and with two-dimensionally distributed heat generations. This mathematical model was implemented to replace conventional finite-elements (FEM) thermal simulators for fast thermal mappings, accurate within 1% and able to run in interaction with electrical and electro-thermal automatic design tools. His convenience in terms of speed and calculation amounts is due to the required 2-D meshing grids only at the interfaces instead of 3-D. The implemented thermal simulation program was validated by comparing the results of some virtual samples with the corresponding temperature and heat flux maps obtained with the FEM analysis. The amount and the origin of the error percentages with respect to the FEM analysis were also investigated as a functions of the free input parameters of the model.

Introduction

The thermal analysis of electronic devices and circuits and their packaging structure can be usually performed using the finite-element based (FEM) thermal simulation, which is a general purpose, widely used and reliable tool also for complex three-dimensional structures. As known, it is based on the discretisation of the thermal conduction equations within a close net of solid elements. Therefore the FEM analysis needs a 3-D meshing of the solid system, which generally is not uniform, so that the model preparation for optimum results may be complex and overall it requires some qualified capabilities by the operator.

Furthermore the heat conduction dissipation properties of a system are usually due to both the device package, assembled by the device manufacturers, and to a second part assembled by the user or the system producer. Therefore the maximum temperature within the devices is caused by two designing steps realized by different industrial subjects, which generally may use different thermal analysis methodologies with different accuracy. Instead the importance of the thermal problem from the reliability point of view, not only for the
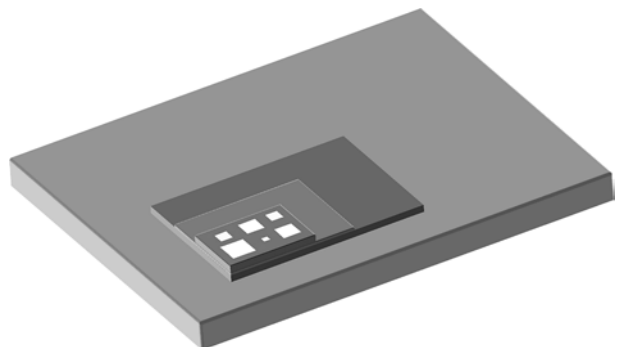

FIG.1 : Planar device with its stacked assembling

electronic device and system producer but also for the manufacturing users, would require less expensive, less time consuming and more easily programmable thermal simulation tools in order to perform fast and equally reliable analyses.

Most of electronic assemblies (both devices and boards), especially for high and very high power handling, can be described by simple structures consisting of stacks of homogeneous layers of different materials and dimensions, directly connected by means of thin soldering or attaching layers. The power dissipation may
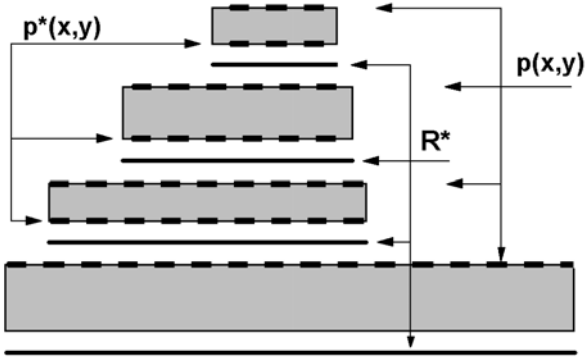
FIG.2 : Exploded cross-section of a stacked mounting and its heat generation and resistive elements.
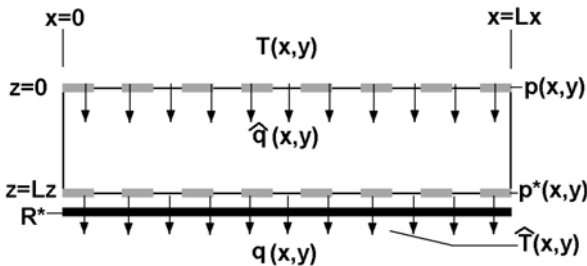

FIG.3 : Thermal parameters in the single-slab case.

be assumed as two-dimensional on one or more interfaces and with the bottom side generally connected to a constant temperature heat sink, directly or through a thermal convection coefficient. These structures, quite similar to an asimmetric step pyramid, are shown in the Fig. 1 as a perspective view.

If the above simple geometrical configuration is suitable to represent the whole assembling structure, the steady-state thermal simulations may be performed using dedicated mathematical models with explicit analytical relationships [1] which can be implemented in faster and easily programmable simulation tools.

The analytical approach to the thermal problem has in general the following advantages with respect to the conventional FEM analysis. As it will be shown later, the analytical model can operate with a 2-D rectangular meshing at the interfaces instead of 3-D volumetric meshing. This implies a decrease of the number of the unknown variables, therefore leading to a shorter computing time. Furthermore, all the 2-D interface grids may be uniform, i.e. composed by square cells with the same area, so that the pre-processing procedure and the model construction can be fully automatic. All these properties make the analytical simulation tool suitable to interact with CAD programs for the design of both electronic devices and system assemblies.

Another important feature is that this tool, thanks to its speed and reduced complexity, is particularly suitable to be used as a thermal solver in cyclic electro-thermal simulation programs based on the mutual interaction between the device electrical characteristics and the temperature distributions. A typical situation needing

this type of tool is the so-called 'hot-spot' phenomenon occurring in high power bipolar transistors [2,3].

In this communication, an analytical thermal simulation tool for the steady-state of electronic systems is presented. In the following it will be addressed as DJOSER model. It can be used for planar electronic systems and it is able to well represent a wide range of electronic assembling configurations such as integrated circuits encapsulated in power packages, flip-chip or BGA mounted devices, hybrid circuits, multi 'naked' chip assemblies, printed electronic boards assembled in surface mounting technology or on multi-layer metal interconnecting substrates. The condition needed is that the active power dissipation must be two-dimensional, not volumetric, and must be located at the top surface or at an interface between two layers. At present, this hypothesis can be taken in the most practical cases of electronic industry. Buried power generations within the body of a die may be modelled by dividing the single slab into two or more layers.

However this model cannot be used, or could be only roughly approximated, when the slabs or the interfaces do not have uniform thermal properties on the horizontal plane or there are some localized dissipating details, as for instance vertical dissipaters, the external pins of an encapsulated integrated circuit, or when the layers in the structure are not homogeneous or their thermal conductivity depends on the horizontal position. An example is the presence of large thermal vias, usually tin filled, connecting two metal planes in multi-layer metal interconnecting substrates. In the following sections the mathematical background of the model is briefly presented and the results of thermal simulation runs on some virtual test structures are shown in comparison with those obtained using the standard FEM analysis. The error differences between the two methods are shown as a function of the input simulation parameters. The main goal of the present work is to achieve thermal evaluation mapping within an accuracy of 1%.

Theory

Fig. 2 shows the physical structure of a stacked assembly with all the thermal elements taken into account by the DJOSER model. This structure looks like a rectangular step pyramid with any degree of asymmetry and with the base in contact with a constant temperature heat sink. 'Step pyramid' means that the lateral sizes of each layer must be larger or equal to those of the layer above and smaller or equal to the sizes of the layer below. Each slab is thermally homogenous and isotropic and may be considered thermally insulated both on the lateral vertical surfaces in contact with the environment and on the top surface not directly connected with the layer above. The thick lines between two adjacent layers in Fig. 2 have the following meanings. The continuous lines marked with the label R* indicate the presence of a zero-thick distributed thermal resistance per unit area (its value is set to zero in the case of not resistive interface), expressed in K/m^2W as the reciprocal of a heat transfer

coefficient and whose value is uniform over the whole interface area. This parameter is able to take into account the thermal effect of soldering or attaching layers which are much thinner than the bulk material slabs. The thermal resistance at the bottom of the lower layer may be also used to take into account an eventual convection heat exchange with the bottom environment.

The dashed lines marked with the label p(x,y) and p*(x,y) represent top or internal active heat generation densities located at any interface, with any continuous distribution or arranged in clusters or heating islands. p(x,y) are the heat generations placed below the contact thermal resistance, while p*(x,y) are placed above it. This second type of heating power density can represent, for instance, the case of a silicon die mounted in flip-chip configuration, in which the electrical power is dissipated on the bottom side of the die, just above the thin underfilling layer.

The problem of heat conduction corresponding to the above-defined boundary conditions is the calculation of the temperature and heat flux distributions at all the interfaces between the layers under the steady-state regime. The resolution of this problem, which is practically an extension and an improvement of other models cited in literature [4,5], is based on the resolution of the single slab whose cross-section is shown in Fig. 3. Its thermal steady-state regime is ruled by the following set of linear equations holding under the hypothesis of adiabatic lateral walls:

$$
\begin{cases}
\nabla^2 T = 0 \\
-k \dfrac{\partial T}{\partial z} = p(x,y) + \hat{q}(x,y) & \text{at } z = 0 \\
-k \dfrac{\partial T}{\partial z} = -p*(x,y) + \dfrac{T - \hat{T}(x,y)}{R*} & \text{at } z = L_z
\end{cases}
\tag{1}
$$

where T is the temperature, k is the thermal conductivity, the functions $\hat{q}(x,y)$ e $\hat{T}(x,y)$ are the top heat flux and the bottom temperature respectively, R* is the contact distributed thermal resistance between this slab and the lower one. The functions p(x,y) e p*(x,y) are also drawn in the Fig. 3. The single slab solution can be obtained by means of the variable separations and superposition techniques, so that the upper temperature at z=0 and the heat flux at z=L_z are expressed by the two following integral relationships:

$$
T(x,y,0) = \int_0^{L_x}\int_0^{L_y} [p(x',y') + \hat{q}(x',y')] \cdot G_{11}(x',y'|x,y)dx'dy' +
$$

$$
+ \int_0^{L_x}\int_0^{L_y} [R*p*(x',y') + \hat{T}(x',y')] \cdot G_{12}(x',y'|x,y)dx'dy'
\tag{2}
$$

$$
q(x,y,L_z) = \int_0^{L_x}\int_0^{L_y} [p(x',y') + \hat{q}(x',y')] \cdot G_{21}(x',y'|x,y)dx'dy' +
$$

$$
+ \int_0^{L_x}\int_0^{L_y} [R*p*(x',y') + \hat{T}(x',y')] \cdot G_{22}(x',y'|x,y)dx'dy'
\tag{3}
$$

The spatial functions G(x',y'|x,y) are Green functions consisting of double harmonic Fourier series [6]. Using the coordinates system shown in Fig. 3, the G functions are just cosine and may be defined as follows :

$$
G_{ij}(x',y'|x,y) =
$$

$$
\sum_{n=0}^{\infty} \sum_{m=0}^{\infty} C_{ij}(n,m) \cos(\beta_n x') \cos(\mu_m y') \cos(\beta_n x) \cos(\mu_m y)
\tag{4}
$$

where $C_{ij}(n,m)$ are suitable coefficients containing the geometrical data of the layer, its thermal conductivity and the eventual bottom contact thermal resistance. The eigenvalues are given by:

$$
\begin{cases}
\beta_n = n\pi / L_x \\
\mu_m = m\pi / L_y
\end{cases}
\quad \text{with} \quad n, m \text{ integer}
\tag{5}
$$

Furthermore, the following relation holds:

$$
G_{12}(x',y'|x,y) = G_{21}(x',y'|x,y)
\tag{6}
$$

If we turn back to the case of a multi-layer step pyramid, it is quite evident that for a single slab of the stack the functions $\hat{q}(x,y)$ and $\hat{T}(x,y)$ are not really known, being the thermal flux coming from the above layer and the temperature distribution of the contact area with the lower layer respectively. Obviously in the top layer of the stack the heat flux is known and it is represented by the function p(x,y), while the corresponding $\hat{q}(x,y)$ is zero. On the other hand the temperature $\hat{T}(x,y)$ at the bottom of the lowest layer is still known and corresponds to the assigned heat sink temperature. Therefore the set of relations (2) and (3) for all the layers are an integral system with 2(Ns-1) equations and 2(Ns-1) unknown variables, Ns being the number of slabs belonging to the whole structure. This is the mathematical core of the DJOSER model.

However, since all the thermal functions are continuous and spatially two-dimensional, the real implementation of the method requires the use of suitable numerical approximations. In equations (2) and (3), by substituting the Green functions with their expression in (4), all the terms of the sums in the second members can also be re-written in the following form:

$$
\sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \Phi(n,m) \cdot Cij(n,m) \cdot \cos(\beta_n x) \cdot \cos(\mu_m y)
\tag{7}
$$

where $\Phi(n,m)$ is given by

$$
\Phi(n,m) = \int_0^{Lx}\int_0^{Ly} \Phi(x',y') \cos(\beta_n x') \cdot \cos(\mu_m y') dx'dy'
\tag{8}
$$

Here the function $\Phi(x,y)$ indicates any of the four involved functions p(x,y), R*p*(x,y), q(x,y) and T(x,y).

The double integrals in equation (8) and (2-3) must be practically calculated by means of two dimensional quadrature formulas. This implies that all the interfaces of

the structure must be divided into regular two-dimensional grids of cells and the continuous functions must be known by means of their values in a rectangular grid: each value (Φi) is relative to the centre of a single cell or to one of its corners depending on the type of quadrature formula chosen. Therefore, equation (8) can be approximated by

$$\Phi(n,m) = \sum_{i=1}^{N} \Phi i \cdot B(n,m) \quad , \quad \Phi i = \Phi(xi, yi) \qquad (9)$$

where N is the total number of cells and B(n,m) is a coefficent which depends on the type of quadrature formula. In particular, if the numerical approximation of the functions is the rectangular one (the function is constant within the cells having 2a and 2b sizes), eq. 9 becomes:

$$\Phi(n,m) = \sum_{i=1}^{N} \Phi i \cdot \int_{xi-a}^{xi+a} \int_{yi-b}^{yi+b} \cos(\beta_n x') \cdot \cos(\mu_m y') dx' dy' \qquad (10)$$

where xi and yi are the coordinates of the centre of the cells.

Using these approximations, the system of equations given by (2) and (3) for the single slab case can be re-written in a compact form as follows which gives the temperature values at z=0 and the flux at z=Lz in any point of the two surfaces respectively.

$$T(x,y,0) = \sum_{j=1}^{N} (Pj + \hat{q} j) \cdot \psi j(x,y) + \sum_{p=1}^{M} (\hat{T}b + R * p * b) \cdot \varphi b(x,y) \qquad (11)$$

$$q(x,y,Lz) = p*b + \sum_{j=1}^{N} (Pj + \hat{q} j) \cdot \varphi j(x,y) - \sum_{p=1}^{M} (\hat{T}b + R * p * b) \cdot \omega b(x,y)$$

where N and M are the total number of grid values in the top and bottom surface respectively. The functions ψj, ϕb, ϕj and ωb are defined by the following relations

$$\psi j(x,y) = \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} C_{11} \cdot Bj(n.m) \cdot \cos(\beta_n x) \cdot \cos(\mu_m y) \qquad (12)$$

$$\varphi b(x,y) = \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} C_{12} \cdot Bb(n.m) \cdot \cos(\beta_n x) \cdot \cos(\mu_m y) \qquad (13)$$

$$\varphi j(x,y) = \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} C_{21} \cdot Bj(n.m) \cdot \cos(\beta_n x) \cdot \cos(\mu_m y) \qquad (14)$$

$$\omega b(x,y) = \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} C_{22} \cdot Bb(n.m) \cdot \cos(\beta_n x) \cdot \cos(\mu_m y) \qquad (15)$$

Here the indices j and b mean that the integrals are done on the upper and lower surfaces respectively.

In the case of a multi-layer structure we can build a set of interlaced equations similar to those in (11), where the temperatures and fluxes are evaluated in the coordinates of the cell grids in every interfaces. Therefore this set of equations constitutes a large linear system where the unknown data to be found are all the values of temperature and fluxes in the cells while the known data are all the heat generation densities data, the heat sink temperature distribution at the bottom of the structure and the heat flux data at the top surface of the first layer which corresponds to the top heat generation if the heat convection exchange is disabled. Therefore the total number Ne of equations and unknown variables is given by the following relationship:

$$Ne = \left[2 \cdot \sum_{i=1}^{Ns} nx(i) \cdot ny(i)) \right] - nx(1) \cdot ny(1) - nx(Ns) \cdot ny(Ns) \qquad (16)$$

where Ns is the number of layers of the structure and nx(s) and ny(s) are the arrays containing the lateral dimensions of the interface cell grids.

The resolution of the linear system yields the knowledge of the temperatures and fluxes at the interfaces only within the point grids defined by the cells. However the temperature and fluxes mapping in any point of the interfaces may be achieved using eq. (11) with any resolution.

The errors in the temperature and flux evaluation are due to the two main numerical approximations. The first source is due to the truncation error of the double sums in eq. (12-15) which can be evaluated only for a finite number of eigenvalues. In the present study we used a square set of eigenvalues, being Nnm a free parameter indicating the maximum number of the indices n an m used for the x-axis and y-axis eigenvalues respectively.

The second source of error is related to the quadrature approximation of the continuous temperature and flux functions and it depends on both the degree of quadrature chosen and on the cell densities in which the interfaces have been divided.

In the following sections the rectangular quadrature approximation was used, beside the Cavalieri-Simpson formulas may also be used in order to decrease the number of cells, the system matrix dimensions and hence the calculation time.

Beside the DJOSER model is here solved under the hypothesis of adiabatic surfaces; nevertheless it can be also used in presence of a convective heat exchange with a given environmental temperature, but only if the convection occurs on the horizontal surfaces in contact with the environment. The lateral sides must be still taken as adiabatic, otherwise the problem becomes again 3-D.

The contribution of the heat convection exchange may be implemented in the following iterative way. In the first step the structure is considered adiabatic and the top conduction flux is equal to the heat generation densities at the top surface or on the uncovered surfaces. The top temperature values are calculated in the standard way. The knowledge of these data and of the environment temperature allows to calculate the convection fluxes. They are subtracted to the top heat generations in order to set the new input conduction thermal fluxes.
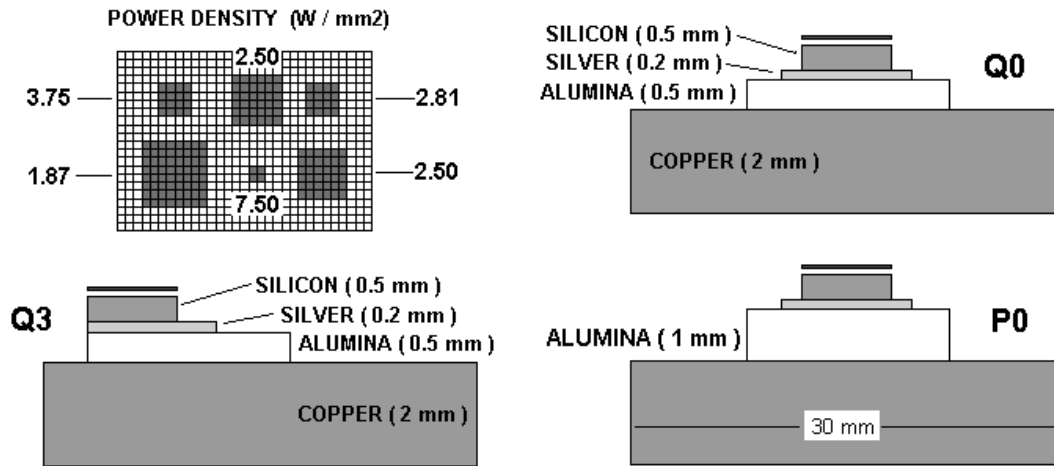
FIG.4 : Surface grid, power distribution (upper left) and cross-sections of the three samples.

The linear system is solved again with the new boundary conditions. Note that the coefficients of the system matrix do not depend on the flux and temperature boundary conditions so that there is no need to recalculate the matrix. This procedure, which easily converges for usual heat convection coefficients, must be stopped when the top temperatures reach stable values.

Test samples

The DJOSER analytical simulation program, implemented in MATLAB 5.0, was tested on a purposely-designed multi-layer model representing an almost typical assembling structure of a packaged power electronic integrated chip. The geometrical and thermal conductivity data of the main sample model (Q0) are shown in the table I.

TABLE I : Numerical data for the sample Q0.

LAYER	k (W/m°C)	Lx (mm)	Ly (mm)	Lz (μm)
Silicon	135	6.2	4.4	500
Silver	419	9	7	200
Alumina	24	14	10	500
Copper	386	30	24	2000

This structure was designed with a sequence of high and low thermal conducting layers in order to test the effects of the different heat flux spreading capabilities induced by different thermal conductivities. The first layer is a rectangular silicon die; the top heat generation density (total power 17.4 W) is organized in square islands, each having its own uniform power density. The whole silicon surface was divided into a grid of 31x22 square cells, 0.2 mm wide. The other layers are a thin and narrow silver conductive film, an insulating alumina slab and a wider copper base acting as a heat-spreading submount. All the top and lateral surfaces were supposed to be adiabatic except the bottom one which is in contact with an ideal heat sink whose temperature was set constant to the value of 0 °C. The other models used for the test simulations were obtained by increasing the thickness of the insulator layer (P0) or inserting a large degree of asymmetry between the layers (Q3). This last geometrical configuration was also used in order to observe the effects on the top temperature distribution of different properties of the lower layers representing the packages or the heat spreaders. Fig. 4 shows the top dissipating power distribution on the clusters and the structure of the basic axisimmetrical model Q0 and the other samples .

In order to establish a reference for the DJOSER result validation, all the designed models were also simulated using the standard and consolidated finite element method performed using the program MARC and the pre-post-processor MENTAT, both by Mac Neal Schwendler Comp. The FEM simulations were carried out using a very dense 3-D meshing grid, (more than 64000 nodes) in order to avoid as much as possible the temperature and flux calculation error with respect to the reality. As an example, the silicon and the silver layers have been modelled using cubic elements with a side length of 0.1 mm, the half of that used by the analytical simulator DJOSER.

Temperature mapping results

Simulation results:

The results of the temperature mapping performed using the DJOSER program are shown in Fig. 5. Here the temperature maps on the top silicon layer for the samples Q0, P0 and Q3 are shown in the same colour scaling. Furthermore, Fig. 6 shows the comparison among the temperature plots of the three samples along the two cross sections shown in Fig. 5 and crossing the points where the higher temperature values occur. As can be seen, the plots in fig. 6 show quite different temperature distributions for the three samples, despite they were obtained with the same heat generation. These differences are due and are
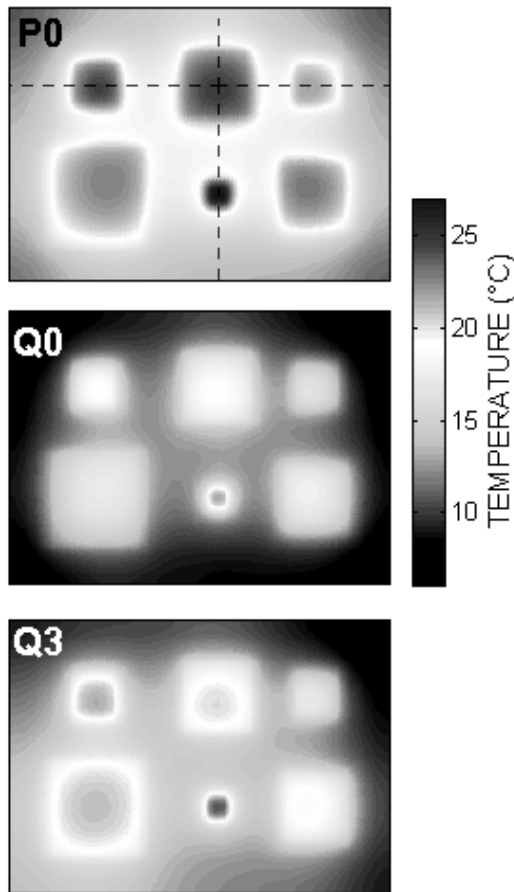
FIG. 5 : Surface temperature maps for the three samples drawn with the same grey color scaling.
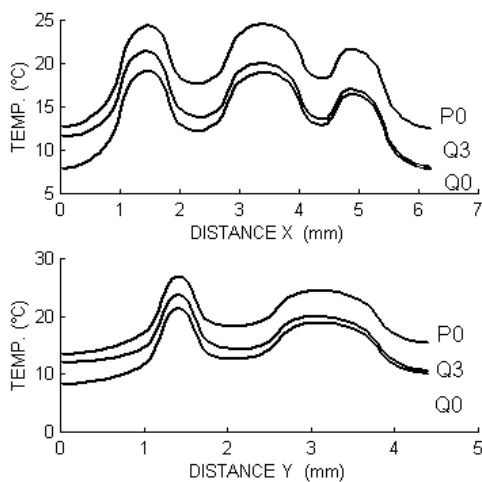

FIG. 6 : Surface temperature plots along the cross sections in the top of Fig. 5 for the three samples.

perfectly consistent with the different geometrical configurations of the layers below the silicon die acting as heat spreaders. In fact, P0 shows a temperature distribution which is quite the same of Q0, but increased by a factor greater than one due to the double thickness of alumina, which is the most thermal resistive layer of the stack. The plots of Q3 show not only an increase with respect of Q0 but also a deformation. In this case

the distortion of the temperature field is quite evident in the left lower corner of the Q3 map in Fig. 5. The different heat flux displacement across the layers is caused by the large asymmetry of the structure which is responsible for this different behaviour. In fact, the location of the upper power source at a corner of a slab, practically avoids the lateral spreading of the heat flux, thus increasing here the upper temperature because of the higher flux concentration. The showed examples testify how the thermal simulation system is well sensitive also to the package geometrical configuration. In Fig. 7 the temperature and heat flux maps at all the interfaces of sample Q0 are also shown in normalized grey scale.

Comparison with the FEM method:

The accuracy of the DJOSER thermal simulation was verified by comparing the silicon surface temperature data with those obtained from the FEM thermal analysis. This comparison is here presented in terms of relative error percentage plots, shown in the Fig. 8, referred to the maximum temperature within the corresponding FEM maps and along the same two orthogonal cross-sections shown in the Fig. 5. All the errors data were obtained by subtracting the temperature values calculated by the DJOSER model in the same nodes of the FEM grid. As can be seen, the error percentage is everywhere within the 1% limit which is just the main goal of the present simulation model.

Despite this good results, it is still necessary to study the accuracy of the model as a function of the simulation parameters and consequently of the calculation time.

Simulation error discussion

The evaluation error on the top surface temperature maps is mainly caused by two different factors: i) the truncation approximation on the infinite harmonic series included in the integral system coefficients (see equations 4 and 12-15) and ii) the quadrature of the temperature and flux functions within the inner surfaces needed for the integral evaluations.

As far as the first cause is concerned, the relationships (12-15) are double infinite harmonic series defined by a two-dimensional unlimited array of eigenvalues βn and μm. These series are typically slowly convergent and the truncation error function has generally a decreasing but irregularly oscillating behaviour. In the present case these series were calculated for square matrices of eigenvalues whose side is defined by the number Nnm. This parameter, which must be separately and differently set for each layer of the structure is one of the free input data of the simulation model. In order to show the typical error behaviour induced by this factor, the temperature error percentage was calculated for a wide range of Nnm in a simpler structure composed by the silicon layer of sample Q0 only, with the same power distribution, and where all the other layers of the stack
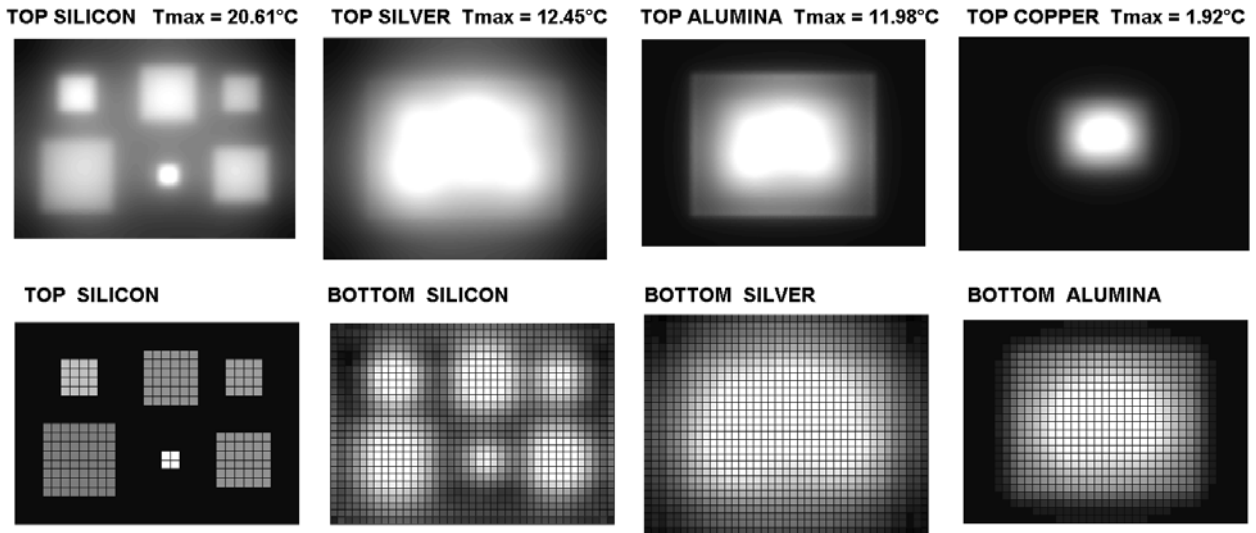
FIG. 7 : Gray-scale maps of temperature (upper row) and heat fluxes (lower row) at the interfaces of sample Q0. In each map the color scale is normalized to its own maximum value. The cell grids are traced in the flux maps.

were replaced by a uniformly convective heat exchange coefficient of suitable value on the bottom side. This model is quite different from the original one and, beside it is very faster, generally leads to a worse accuracy greater than 6%, due to the lack of information about the internal heat flux displacement. However it allows us to verify the error function for a single layer and in a single point of the silicon surface using a very high number of eigenvalues.

Fig. 9 shows the plots of the error percentage as a function of Nnm and calculated in two single points of the surface: the centre (curve A) and the border (curve B) of the smallest dissipation island. In multi-layer cases, the total error in the temperature evaluation is due to the superposition of the series truncations in each slab. In order to study the cumulative effect on the truncation error, many simulation runs were carried out on a two-layer structure, composed by a square silicon
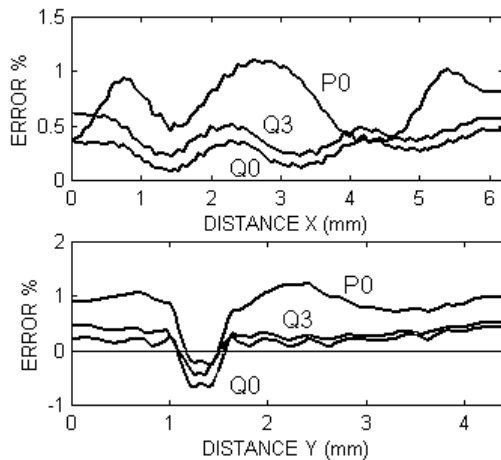
die on a larger aluminium slab (see top of Fig. 10), changing the values of the parameter Nnm (equal for the two layers) in the range 30-110. The simulations results are showed in the Fig. 10 in term of bar diagrams of the average absolute error percentage and maximum absolute error percentage over the whole silicon surface. As can be seen, in the bar diagram the height of the bars is not monotonically decreasing with increasing Nnm as expected, but it has higher peaks caused by the irregular and oscillating nature of the truncation error. Those cases probably correspond to the situation in which the errors in all the layers have the same sign, so that the algebraic averaging effect does not occur.

The second cause of error in the temperature evaluation is due to the discretisation of the 2-D temperature and flux functions into a regular matrix of values relative to the centre of the cells. The cell sizes influence the accuracy of the integral calculations. Furthermore the error due to the function discretisation generally depends on the local

FIG. 8 : Relative error percentage plots of the DJOSER simulations with respect to the corresponding FEM data along the cross sections of Fig. 5.
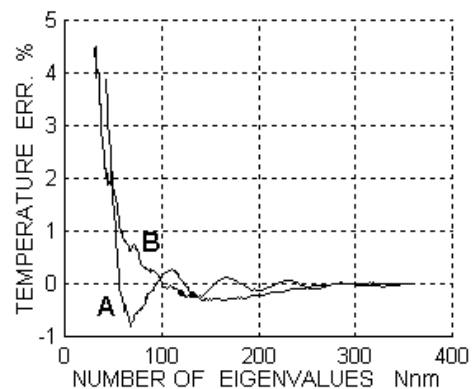

FIG. 9 : Error percentage plots for a single layer structure (silicon) as a function of the maximum number of eigenvalues per series. A) centre of the smallest cluster; B) boundary of the same cluster.
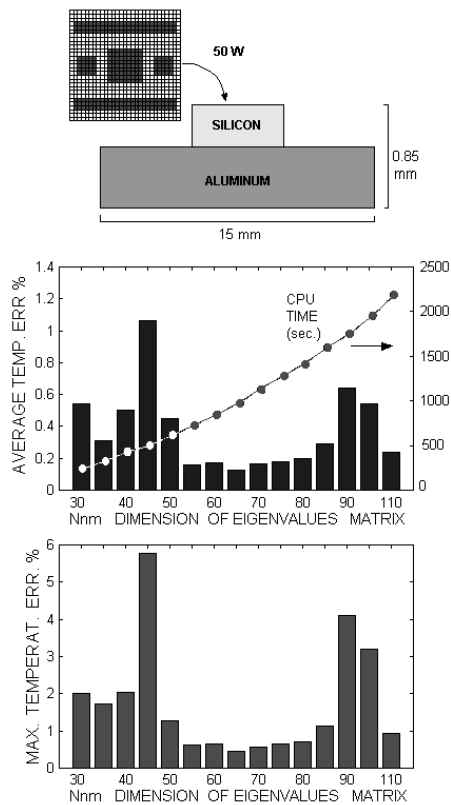
FIG. 11 : Average and maximum error for the two-layer structure versus the number of cells per side. The total calculation time is also shown.

FIG. 10 : Average and maximum error for the two-layer structure shown above, as a function of the parameter Nnm. The total calculation time is also shown.

gradients. The use of a not uniform cell grid, denser where high temperature variations occur, may be useful to better dominate this error, but in this way the model construction and pre-processing would be more complicate and the easy preparation advantage of the DJOSER model would be lost. On the other hand, the decreasing of the number of cells in the interfaces without active power dissipation implies the total calculation time decreasing. The effect of this second type of error can be seen in the Fig. 11, which shows the relative error percentage calculated in several runs of simulation performed on the same sample. In the samples, the number of cells per side (nx=ny) on he bottom of the two layers was changed in the range 5-43, taking constant the cell density of the top silicon surface where the power is dissipated. These second couple of bar diagrams show a quite regularly decreasing behaviour with increasing cell density except a small peak occurred in the middle of the range, perhaps due to a sort of resonance with the chosen value of the maximum number of the eigenvalues used.

In the Figs 10 and 11, the plots of calculation times on a Pentium 4 (1.5 Ghz) personal computer are also reported. However these data cannot be directly used for speed performance comparison with the FEM analysis. This is because at present the DJOSER program was not yet compiled, working as interpreted MATLAB routine and further work has to be done in the improvement of the programming structure for increasing speed. Furthermore most (about 75%) of the CPU time is
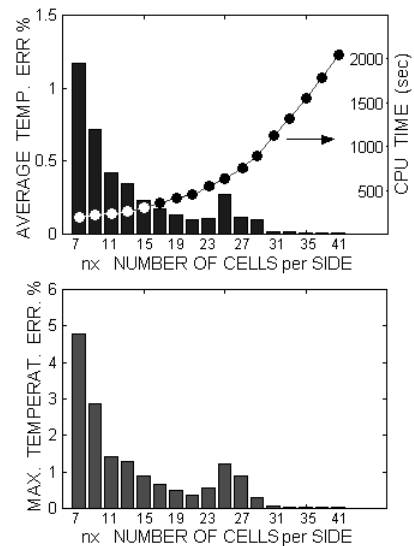
devoted to the construction of the linear system matrix coefficients which do not depends on the boundary conditions: In fact, the coefficients matrix can be stored and used for other simulations with different heat source distributions and boundary conditions. However, taking into account an average speed increase due to the compilation of the routines and on the basis of a rough and provisional estimation, the DJOSER working time is about less than 10% of the time used by the FEM analysis. The employed memory dimension is also reduced by about the same factor.

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