Experimenting with Formal Verification and Model-based Development in Railways: the case of UMC and Sparx Enterprise Architect

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(FMICS 2023)





We are hiring!

- The Formal Methods and Tools (FMT) lab of the Institute of Information Science and Technologies (ISTI) of the Italian National Research Council (CNR) offers two temporary positions for research in the field of formal modelling and analysis of critical software systems, in particular but not limited to the railway and service computing domains.
- Contact us:
 - <u>maurice.terbeek@isti.cnr.it</u>
 - <u>davide.basile@isti.cnr.it</u>

Overview

- Formal Methods in Railways, Model-based Development
- Sparx Enterprise Architect, UML Model Checker
- Mapping of Sparx EA and UMC models
- Case Study: RBC2RBC handover
- Conclusion

Introduction

- Formal methods in Railways
- Model-based Software/Systems Development (MBSD)
 - mainly based on the OMG UML Standard
- Integration of Formal Methods into MBSD
- Survey on formal verification of UML SM [1]
 - "counterexamples are rarely mapped back to the original models"
 - "UMC could be used to verify UML models"
- Integration of UMC with Sparx EA

MBSD, Sparx Enterprise Architect

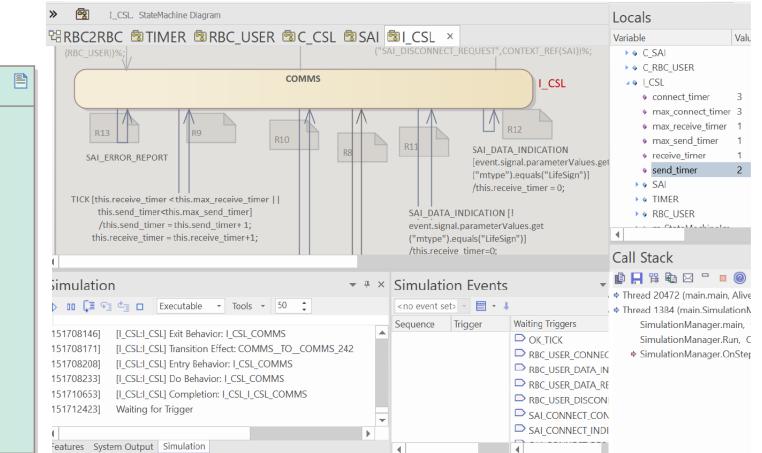
- Development process guided by *models*
- UML: object-oriented paradigm
- State machines: classified behaviour of a class
 - Labels of transitions: trigger[conditions]/effects
- Sparx EA: model-based tool based on OMG UML
- Selected within the H2020 Shift2Rail 4SECURail project based on different criteria
 - e.g., composition of state machine

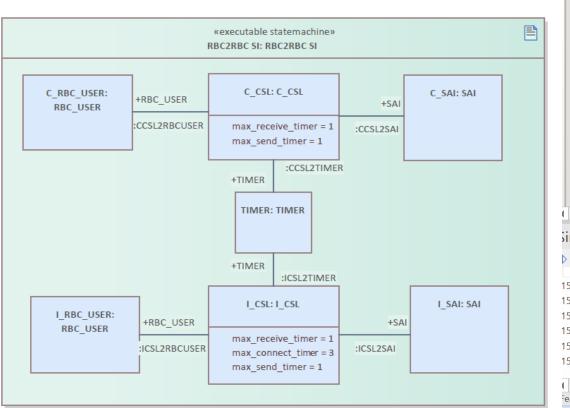
Senterprise Architect



- Executable State Machines
 - Composition of State Machines,
 - Simple instruction for interactions
- Compiled into code for simulation

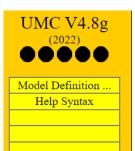






UML Model Checker (UMC)

- Freely available at <u>https://fmt.isti.cnr.it/umc/V4.8/umc.html</u>
- Currently maintained by Franco Mazzanti
- Oriented towards fast prototyping
- Verification of CTL properties of SM
- On-the-fly model checking [1]
- Automatic translation to [2]:
 - LOTOS NT, ProB
 - Formally verified translation



Ouit

Welcome to UMC

UMC is a verification framework developed at the FM&&T Laboratory of ISTI-CNR for the definition, exploration, analysis and model checking of system designs represented as a set of (UML) state machines. Starting with the selection of the "Model Definition ..." command on the left it is possible to browse examples of system designs or experiment with the creation and analysis of new models. The available documentation about this framework (see the provided links) is unfortunately not very recent, but we hope to fix the gap in a near future. In the meanwhile, the online <u>Syntax Help</u> and the interactive syntax driven model editing feature allow to get a partial but still meaningful idea of the supported constructs.

Documentation The Structure of UMC Models (vers. 3.7) The Structure of UMC Logics(vers. 3.3) ... other ...

Download:

A binary distribution of the command-line oriented version of UMC for Linux/ SunSparc/ Windows/ Mac OSX is available. The full framework (http server code + binaries) for MacOS is also available upon request, also in the form of a desktop MacOS application. A selection of deprecated legacy version of UMC are still <u>accessible online</u>.

Requirements: Any modern browser with javascript, HTML5 and SVG support.

Author/Contact/Support: Credits:

Franco Mazzanti franco.mazzanti@isti.cnr.it <u>http://fmt.isti.cnr.it/~mazzanti</u> Graphics generated with GraphViz (<u>http://www.graphviz.org/</u>) Graph minimization with ltsconvert of the MCRL2 toolset (<u>http://mcrl2.org/</u>) Text editing supported by ACE (<u>http://ace.ajax.org</u>) Software developed with Adacore Gnat Ada (<u>http://www.adacore.com</u>)

Sample Code:

Some examples of UMC models

Support and Bug Reports:

franco.mazzanti@isti.cnr.it

[1] F. Mazzanti et al.: A state/event-based model-checking approach for the analysis of abstract system properties. Sci. Comput. Program. 76(2)
 [2] F. Mazzanti et al.: Formal Modeling and Initial Analysis of the 4SECURail Case Study. MARS@ETAPS 2022

Bidirectional Approach UMC SM ↔ Sparx EA SM

Syntactic Restrictions on UML State Machines

- no entry, exit, or do behaviour is present in the states of the model (these behaviors can be equivalently expressed in state transitions),
- interaction happens using only $\mathit{signals},$ and no operation calls are used,
- only one-to-one interactions are used, i.e., no signals broadcast,
- conflicts in enabled transitions are only allowed in the environment,
- no timing behaviour is present (time elapsing is explicated using a TICK event), no internal and local transitions are used, no hierarchical states are used, no history, fork, join and choice nodes are used.

Semantics correspondence

- Sparx State Machines do not have a formal semantics
- No state-space generation in Sparx EA
- Manual inspection of the engine code of ESM:
 - FIFO order of events
 - Deterministic model (no conflicts in enabled transitions)
 - Fixed scheduling of SM
- Semantics of Sparx EA *included* in the semantics of UMC
- Mapping of traces

Environment: Interactive Simulation vs Model Checking

Interactive simulations: the human user acts as the environment.

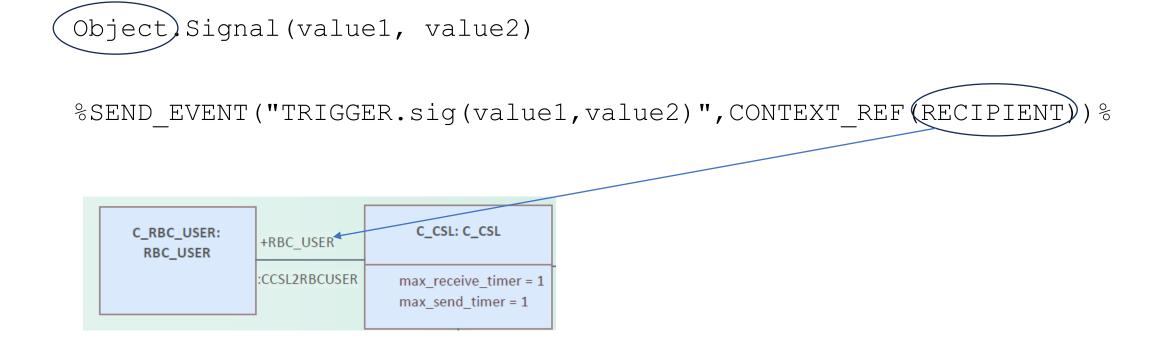
No automation.

Model checking: the environment is explicitly modelled

> to obtain a fully closed system on which the verification is automatic.

Rules for relating the model

- classes have a relation "has-a" with other classes,
 - every object has a reference to other objects to whom it is interacting with



Rules for relating the model

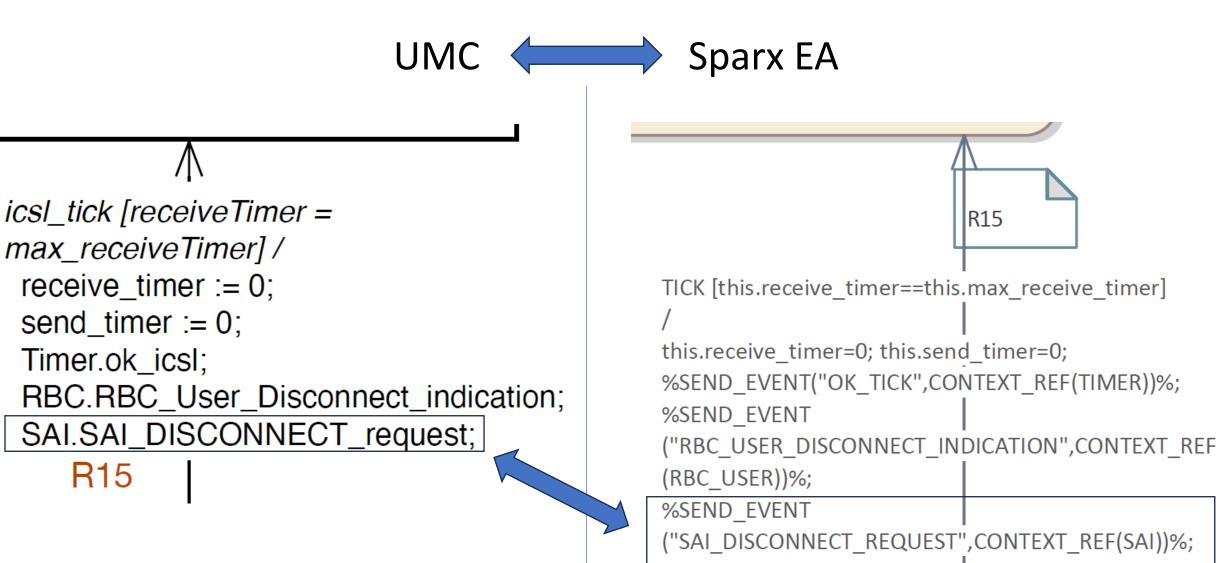
- Signals that are attributes of each class in UMC are in correspondence with global trigger events in the Sparx type Signal and have the same parameters as in UMC.

Object(Signal)value1, value2)

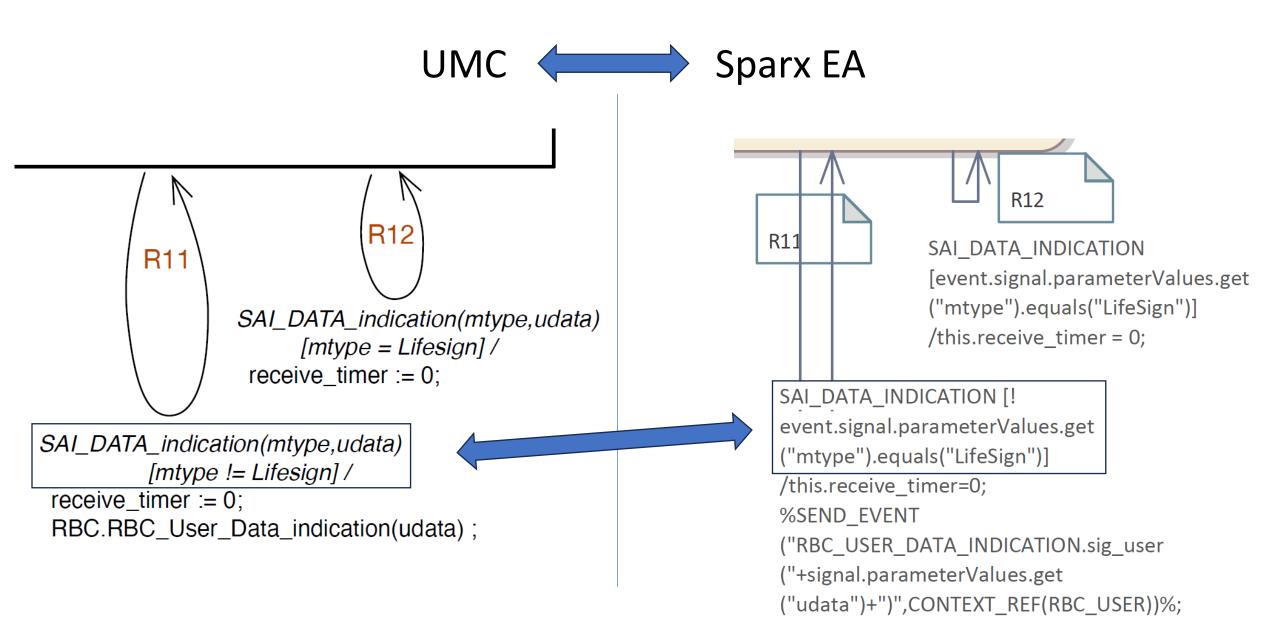
%SEND_EVENT("TRIGGER.sig(value1, value2)", CONTEXT_REF(RECIPIENT))%



Send/write message

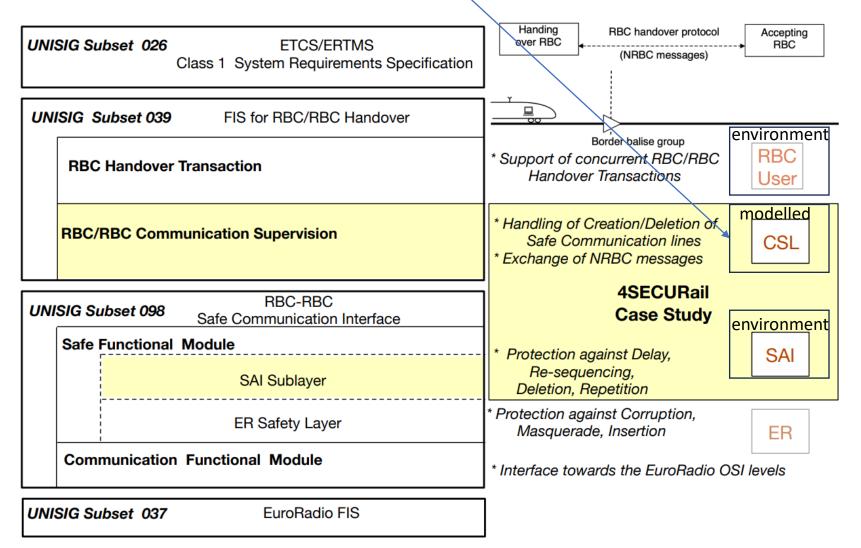


Receive/read message



Case Study: Communication Supervision Layer (CSL)

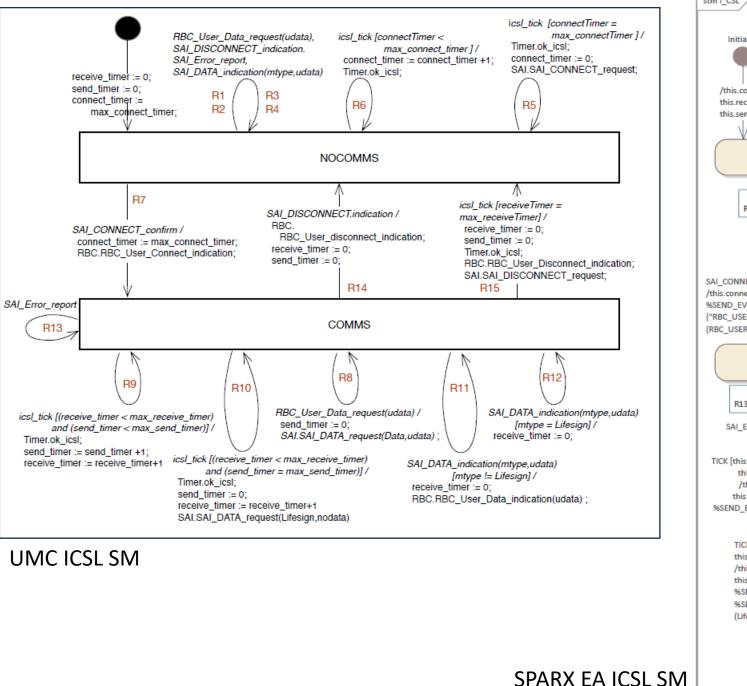
- RBC/RBC handover protocol (borrowed from the 4SECURail project)
- CSL responsible for:
 - opening/closing a communication
 - maintaining connection through life signs

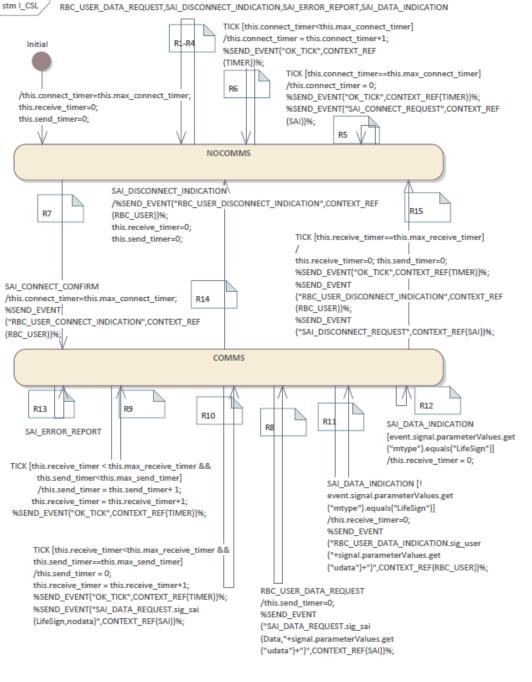


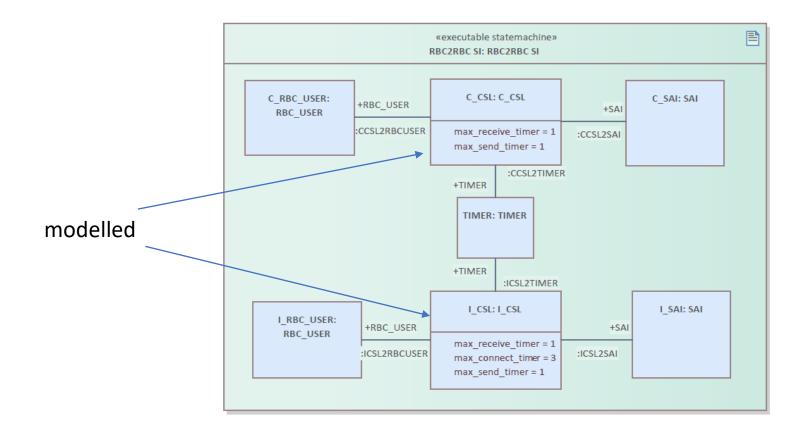
D. Basile et al.: Formal Analysis of the UNISIG Safety Application Intermediate Sub-layer - Applying Formal Methods to Railway Standard Interfaces. **FMICS 2021** F. Mazzanti et al.: Formal Modeling and Initial Analysis of the 4SECURail Case Study. MARS@ETAPS 2022

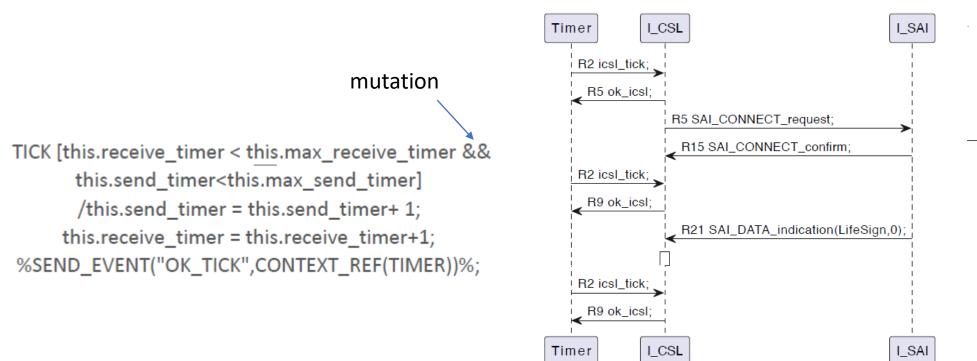
F. Mazzanti et al.: A Case Study in Formal Analysis of System Requirements. SEFM Workshops 2022

F. Mazzanti et al.: The 4SECURail Formal Methods Demonstrator. RSSRail 2022



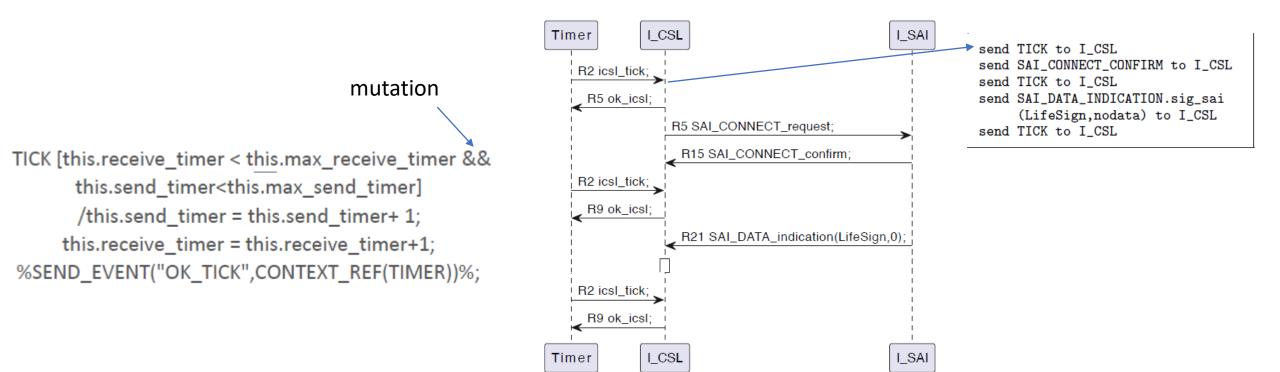




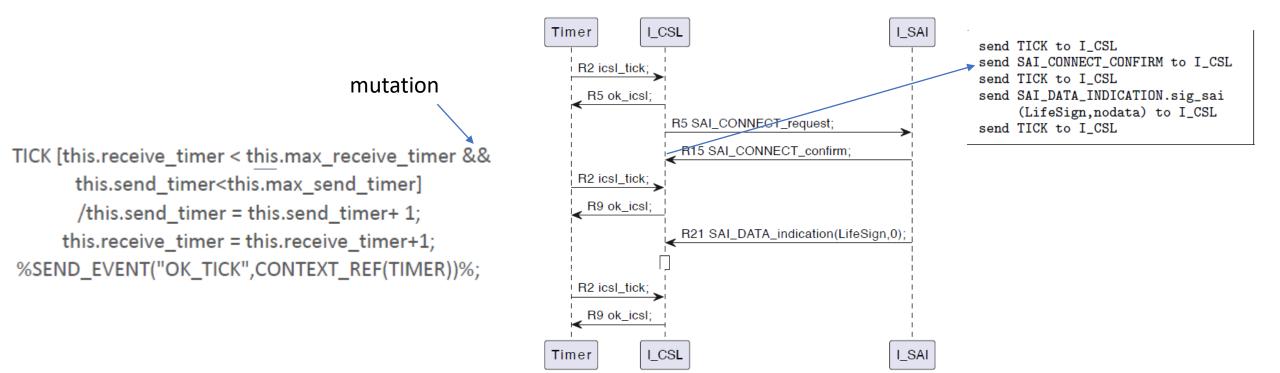


send TICK to I_CSL send SAI_CONNECT_CONFIRM to I_CSL send TICK to I_CSL send SAI_DATA_INDICATION.sig_sai (LifeSign,nodata) to I_CSL send TICK to I_CSL

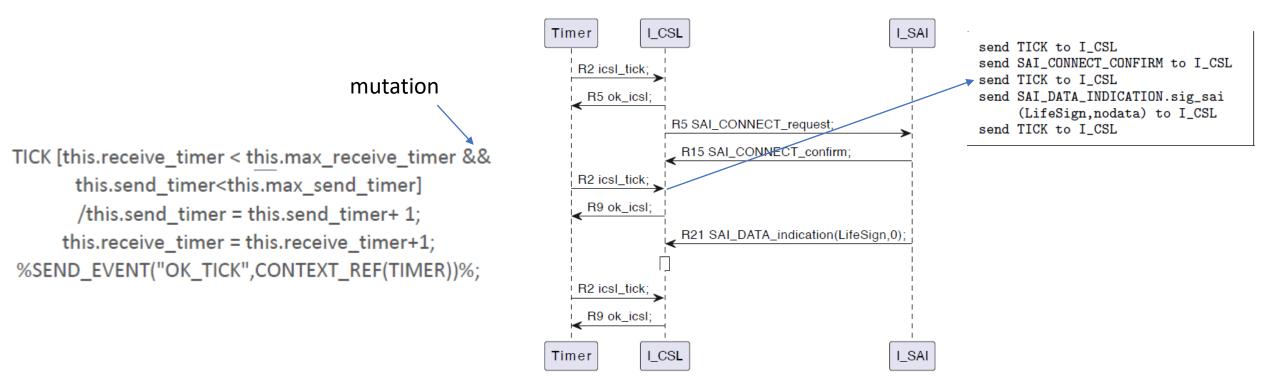
Abstractions {State: ICSL.sendtimer > ICSL.maxsendtimer -> sendTimerError}



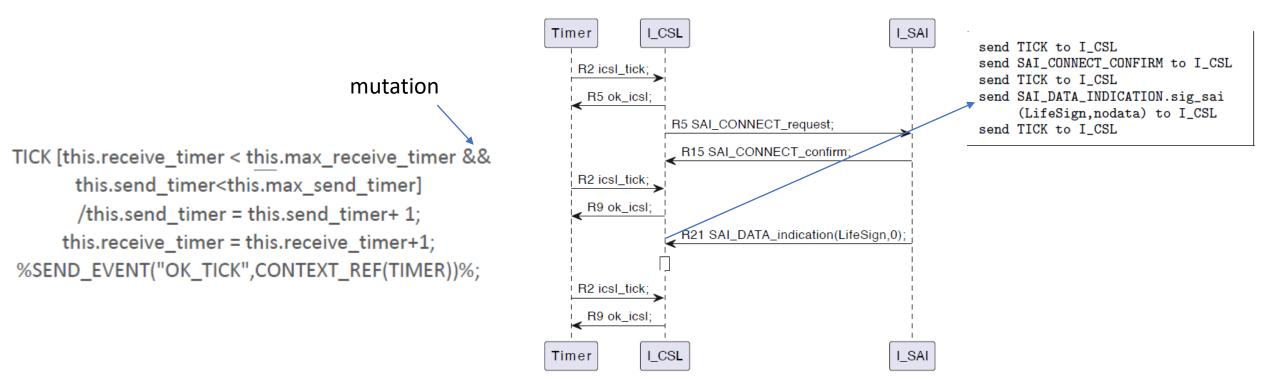
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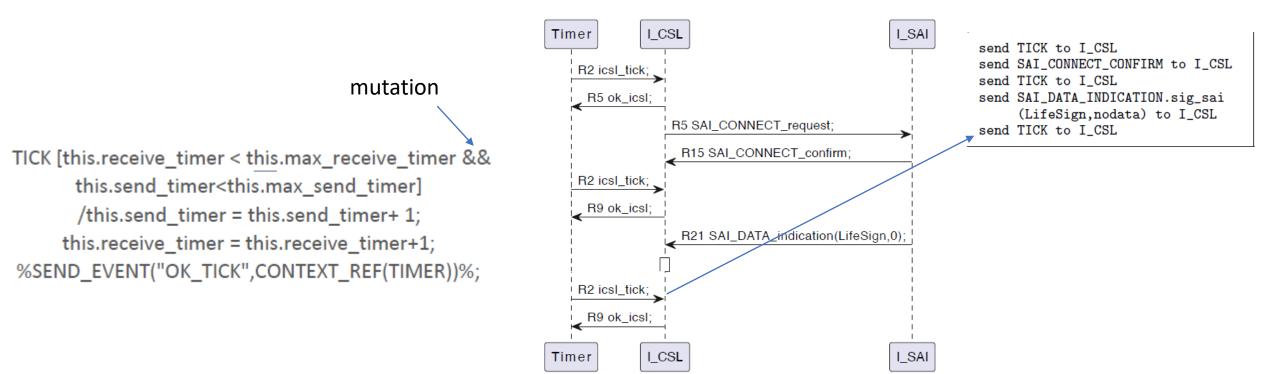
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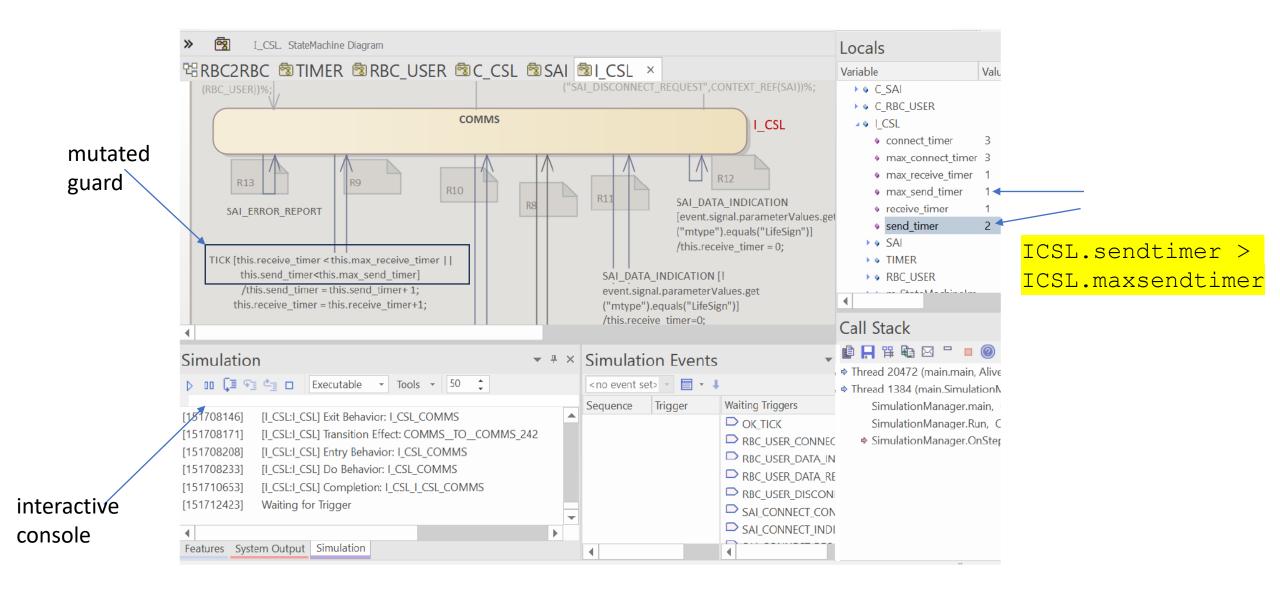


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Model Definition	905 906 Objects:						
Help Syntax	907						
	908 LifeSign, Data: Token; 909 910 I_RBC_User: I_RBC_User (CSL -> I_CSL); 911						
Load the Model	912 I_CSL: I_CSL (R8C_User -> I_R8C_User, SAI -> I_SAI, 913 max_receive_timer -> 3, max_send_timer -> 1, 914 max_connect_timer -> 4, connect_timer -> 4);						
	915 916 I_SAI: I_SAI (CSL -> I_CSL, NSAI => C_SAI, N=> 2); 917						
	918 C_SAI: C_SAI (CSL -> C_CSL, NSAI -> I_SAI, N=> 2); 919 920 C_CSL: C_CSL (RBC_User -> C_RBC_User, SAI -> C_SAI,						
	<pre>921 max_receive_timer -> 3, max_send_timer -> 1); 922</pre>						
Welcome	923 C_RBC_User: C_RBC_User (CSL -> C_CSL);						
Quit	924 925 Timer: Clock (01 -> I_RBC_User, 02 -> I_CSL, 03 -> I_SAI,						
	926 04 -> C_SAI, 05 -> C_CSL, 06 -> C_RBC_User); 927						
8 2 7 8 8	928						
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	931						
	932 Abstractions { 933 TLABELS						
Kandinsky 1908	934 Action: lostevent(\$1) -> lostevent(\$1)						
Tellousky 1900	935 Action: \$1(\$*) -> \$1(\$*) 936 State: I_CSL.send timer > I_CSL.max_send timer -> sendTimer_Error						
	937 }						
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	940 PROPERTIES: EF (sendTimer_Error)						
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Abstractions {State: ICSL.sendtimer > ICSL.maxsendtimer -> sendTimerError}

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UMC V4.8f	The formula: EF sendTimer_Error is FOUND_TRUE in State C1							
Model Definition Help Syntax Edit Model Explore the Model Draw Abstract L2TS Draw Abstract Traces Verify Explain Welcome Quit	This happens because, after the path: C1. Timer \rightarrow C2 {R1_Timer_irbc_tick} C2. I_RBC_User \rightarrow C3 {R1_IRBC_Timer_okirbc} C3. Timer \rightarrow C4 {R2_Timer_icsl_tick} C4. I_CSL \rightarrow C5 {R5_ICSL_Timer_okirsl_ISAI_connectrequest} C5_I_SAI \rightarrow C6 {R7_ISAI_CSAI_sacconnrequest} C6_C_SAI \rightarrow C7 {R6_CSAI_ISAI_sacconnrequest} C6_C_SAI \rightarrow C7 {R6_CSAI_ISAI_sacconncetindication} C7_I_SAI \rightarrow C8 {R15_ISAI_ICSL_saiconnectindication} C9_I_RBC_User \rightarrow C10 {R2_IRBC_discard_connectindication} C10_C_CSL \rightarrow C11 {R8_CCSL_CRBC_rbcuserconnectindication} C11_C_RBC_User \rightarrow C12 {R2_CRBC_discard_connectindication} C12_Timer \rightarrow C13 {R3_Timer_isai_tick} C13_I_SAI \rightarrow C14 {R16_ISAI_Timer_okisa1} C15_C_CSL \rightarrow C17 {R4_Timer_csl_tick} C15_C_CSL \rightarrow C17 {R4_Timer_csai_tick}							
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Conclusion

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 - Notation restrictions
 - Translation Rules
 - Semantics correspondence
 - The output of the formal verification is traced back to Sparx EA
- Lessons learned and limitations
- Future work:
 - full implementation of an application that is formally verified using the proposed methodology.



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- <u>https://twitter.com/davidebasile</u> (video of the presentation)
- Thanks for your attention!