Consiglio Nazionale delle Ricerche

ISTITUTO DI ELABORAZIONE DELLA INFORMAZIONE

PISA

Microfotometro MFA/36

Manuale tecnico

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MICROFOTOMETRO MFA/36

Manuale tecnico

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Sommario

1. Descrizione generale

1.1 Schema a blocchi

La fig. 1.1 mostra lo schema a blocchi dell'MFA/36.

I comandi forniti dal calcolatore sono inviati attraverso il connettore di I/O alla scheda di controllo E; la scheda decodifica i comandi e invia:

- i comandi di moto alla scheda attuatore G che pilota il motore M
- i comandi di lettura al sensore C, attraverso la scheda D; la scheda D provvede a sincronizzare il comando di lettura col ciclo interno della circuiteria del sensore optoelettronico, a convertire in forma digitale su 8 bit i valori analogici dei segnali di campionamento e inviarli al calcolatore ospite tramite il connettore di I/O.

Nello schema sono indicati anche gli alimentatori P1, P2 e T che forniscono le tensioni necessarie per i vari componenti.

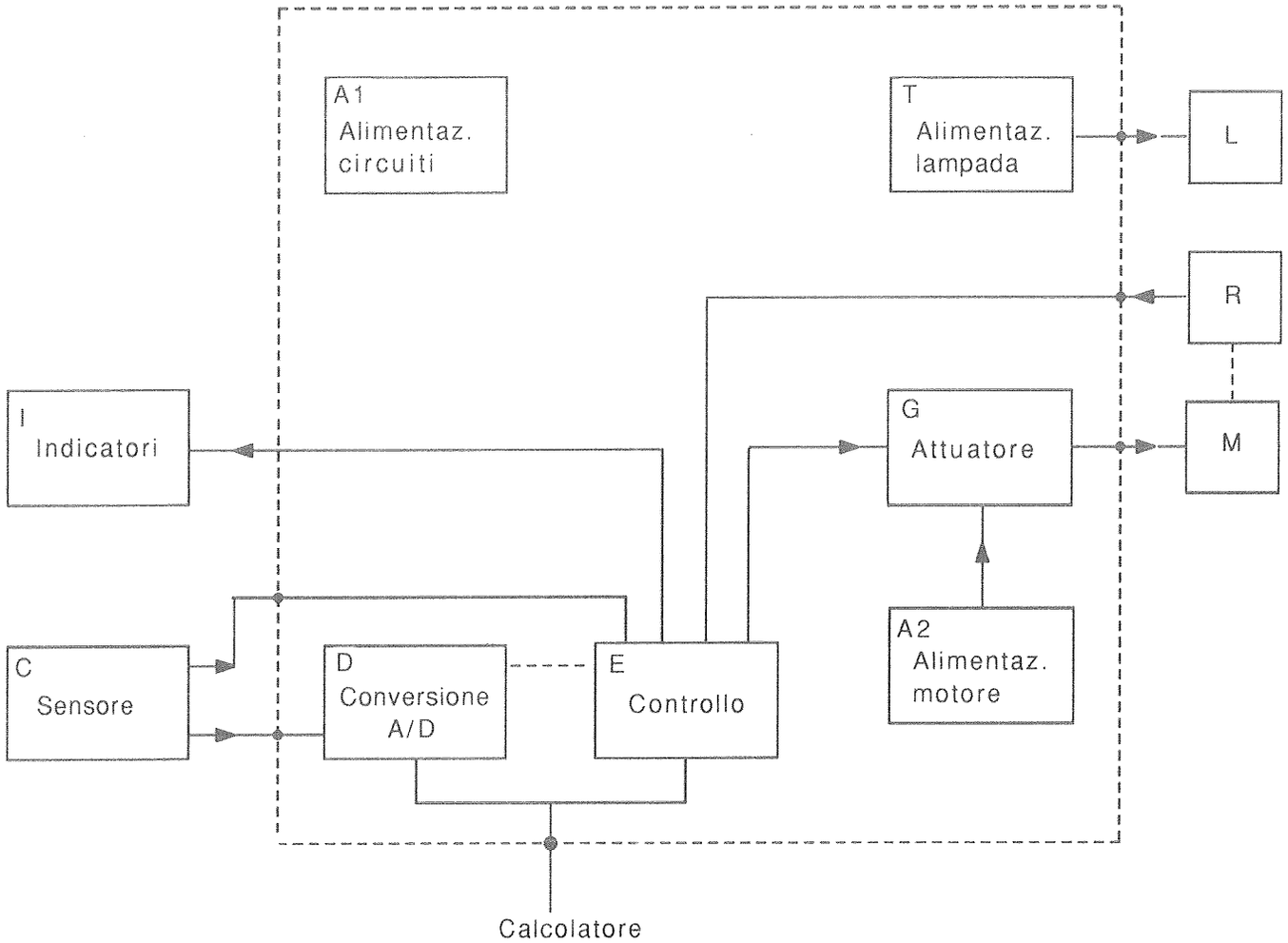


Fig. 1.1 - Schema a blocchi

Componenti dello schema a blocchi

I - Indicatori di stato

C - Sensore optoelettronico RC1024H/RC2048H e schede di pilotaggio RC100B + RC108

D - Conversione segnale video/dato digitale su 8 bit

E - Circuiti di controllo

G - Attuatore per il pilotaggio motore p.p.

L - Sorgente luminosa, lampada alogena 12V, 50/100W

M - Motore per la scansione meccanica sull'asse y: Crouzet 89903001, 4 fasi 200 passi/giro

R - Rivelatori di fine corsa

A1- Alimentatore stabilizzato per circuiteria (5V, ±15V) Power-one HTAA-16W

A2- Alimentatore per motore/attuatore

T - Trasformatore 12V 8A per alimentazione lampada

2. *Descrizione dei connettori*

La figura 2.1 mostra la dislocazione dei connettori dell' MFA/36; il maggior numero di essi è montato sulla faccia posteriore del cassetto portaelettronica, accessibile alzando la parete posteriore dell'apparecchio; gli altri connettori sono montati all'interno del cassetto.

Le pagine seguenti contengono la descrizione dei connettori; per ciascuno di essi sono indicati il nome del connettore, il numero del piedino, il segnale sul piedino, il verso entrante o uscente.

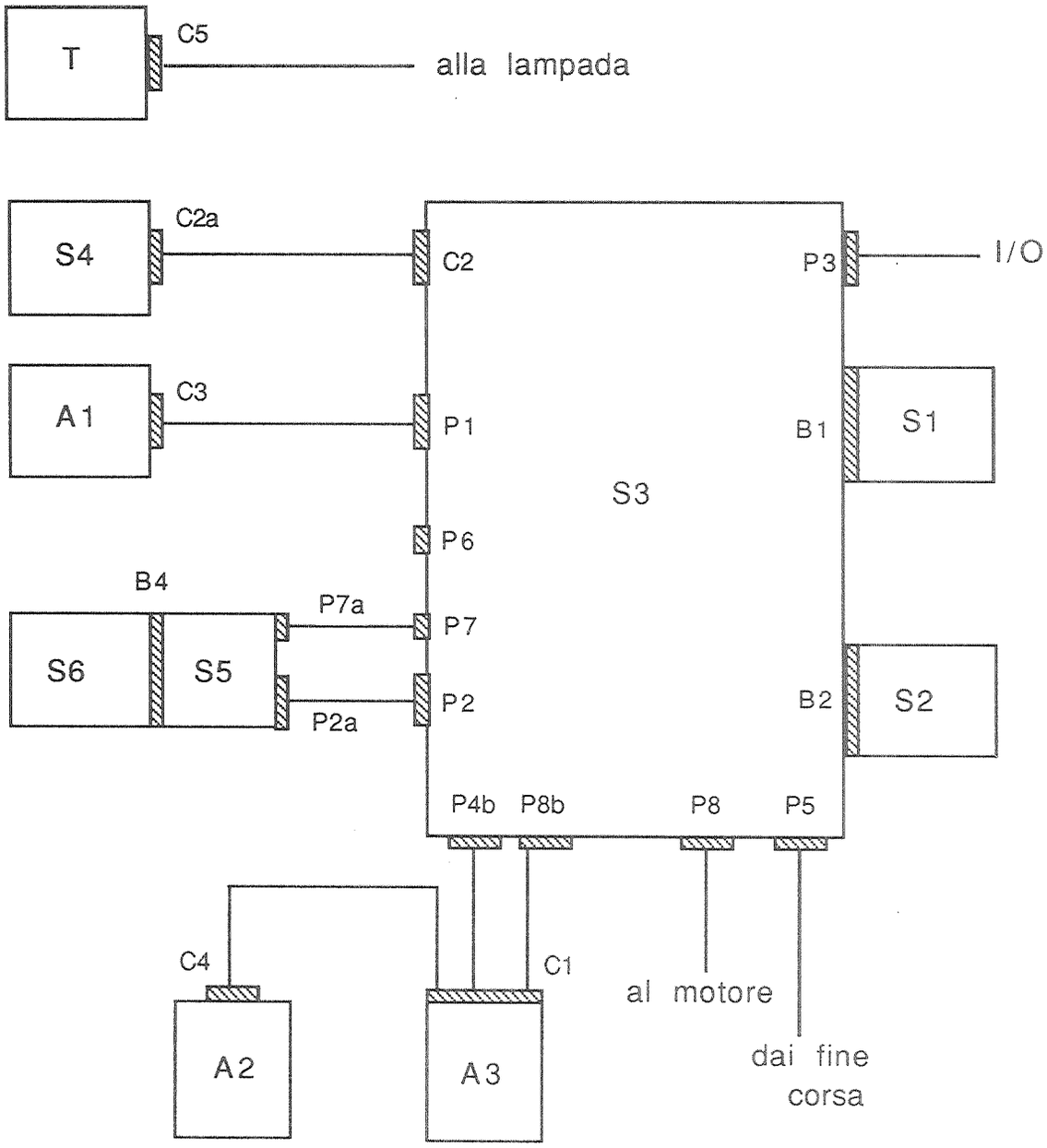


Fig. 2.1 Dislocazione dei connettori

Elenco componenti

T	Trasformatore 160 VA, 2x12V per lampada alogena	
A1	Alimentatore per circuiti digitali	
A2	Alimentatore per motore	
A3	Attuatore per motore	
S1	Scheda MFA B1	conversione A/D
S2	Scheda MFA B2	controllo
S3	Scheda MFA B3	master
S4	Scheda MFA B4	indicatore
S5	Scheda MFA B5	adattatore
S6	Scheda B4	Reticon RC100

Lista delle sigle

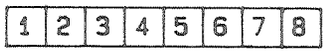
+5, +5v	alimentazione in continua, volt
+12, +12v	alimentazione in continua, volt
+15, +15v	alimentazione in continua, volt
-15, -15v	alimentazione in continua, volt
A/I	comando per la direzione di moto
Analog In	impulso per segnale video del sensore
Blank	impulso di fine riga del sensore
Clock	impulso di sincronismo di cella del sensore
Data 0-7	bit del dato di lettura (MSB, bit più significativo)
DC	Device Command; sincronismo dei comandi
DF	Device Flag; risposta del dispositivo
EOF	sincronismo di fine conversione A/D
FCI, FCA	Fine Corsa Indietro, Avanti del carrello motore
GND	massa
Impulso moto	impulso di pilotaggio dell'attuatore motore
φ 1-4	fasi di pilotaggio del motore
L, Lett	comando di lettura
M, Moto	comando di avanzamento motore
Passo	impulso di avanzamento
Start C	impulso di inizio conversione A/D
Start	impulso di inizio riga del sensore
V+	alimentazione comune motore p.p.
Video	segnale video del sensore

Elenco connettori

Sigla	Tipo
P1	Morsettiera 8 contatti
P2	DIP 16 contatti
P2a	DIP 16 contatti
P3	Cannon PIN 37, maschio
P4	Cannon PIN 9, maschio
P4b	Morsettiera 4 contatti
P5	Cannon PIN 9, femmina
P6	BNC 2 contatti
P7	BNC 2 contatti
P7a	BNC 2 contatti
P8	Cannon PIN 15, femmina
P8b	Morsettiera 8 contatti
B1	Spina 22+22 contatti
B2	Spina 22+22 contatti
B4	Spina 22+22 contatti
C1	Morsettiera 12 contatti
C3	Morsettiera 5 contatti

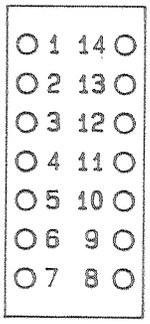
Piedini	Segnale	Note	
1	+5V	← rosso	C3-2
2	+5V	← rosso	C3-2
3	+15V	← giallo	C3-5
4	+15V	← bianco	C3-5
5	-15V	← verde	C3-3
6	-15V	← verde	C3-3
7	GND	marrone	C3-1
8	GND	nero	C3-1

Connettore P1



Piedini	Segnale	Note
1	Start	← P2a,1
2	Blank	← P2a,2
3	Clock	← P2a,3
4		
5	+5V	→ P2a,5
6	+5V	→ P2a,6
7		
8	-15V	→ P2a,8
9	GND	
10	GND	
11	GND	
12	GND	
13	GND	
14	GND	
15	GND	
16	GND	

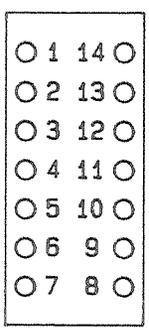
Connettore P2



DIP/16

Piedini	Segnale	Note
1	Start	← B4,B
2	Blank	← B4,D
3	Clock	← B4,5
4		
5	+5V	→ B4,E
6	+5V	→ B4,E
7	+15V	
8	-15V	→ B4,Y
9	GND	
10	GND	
11	GND	
12	GND	
13	GND	
14	GND	
15	GND	
16	GND	

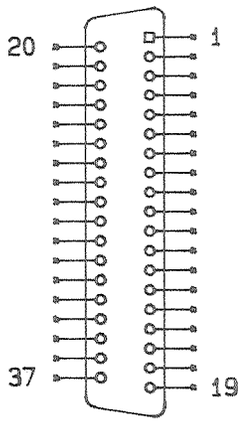
Connettore P2a



DIP/16

Piedini	Segnale		Note	
1				
2				
3	DATA 7	MSB	←	B1-B
4	DATA 6		←	B1-C
5	DATA 5		←	B1-D
6	DATA 4		←	B1-E
7	DATA 3		←	B1-F
8	DATA 2		←	B1-H
9	DATA 1		←	B1-J
10	DATA 0		←	B1-K
11	DF		←	B1-L
12	FCI		←	P5-1
13	FCA		←	P5-2
14	Lettura		→	B2-6
15	Moto		→	B2-4
16				
17	A/I		→	B2-5
18	DC		→	B2-3
19				
20-37	GND			

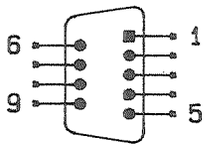
Connettore P3



CANNON 37 PIN

Piedini	Segnale	Note
1	Impulso moto	→ P4b-1
2	A/I	→ P4b-2
3	GND	
4		
5		
6		
7		
8		
9	GND	

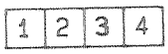
Connettore P4



CANNON 9 PIN

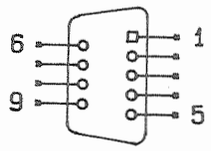
Piedini	Segnale	Note		
1	Impulso moto	→	verde	C1-5
2	A/I	→	celeste	C1-3
3	GND	→	bianco	C1-4
4	GND			

Connettore P4b



Piedini	Segnale	Note
1	FCA	← bianco
2	FCI	← marrone
3		
4		
5		
6	GND	
7	GND	
8	GND	
9	GND	

Connettore P5



CANNON 9 PIN

Piedini	Segnale	Note
1	Start	
2	GND	

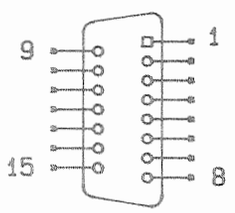
Connettore P6

Piedini	Segnale	Note
1	Video	
2	GND	

Connettore P7; P7a

Piedini	Segnale		Note	
1	φ1	A	←	P8b-6
2	φ1	A	←	P8b-6
3	φ2	$\bar{A}$	←	P8b-7
4	φ2	$\bar{A}$	←	P8b-7
5	φ3	B	←	P8b-1
6	φ3	B	←	P8b-1
7	φ4	$\bar{B}$	←	P8b-2
8	φ4	$\bar{B}$	←	P8b-2
9				
10	V+	A	←	P8b-5
11	V+	A	←	P8b-5
12	V+	A	←	P8b-5
13	V+	B	←	P8b-3
14	V+	B	←	P8b-3
15	V+	B	←	P8b-3

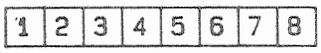
Connettore P8



CANNON 15 PIN

Piedini	Segnale		Note		
1	φ3	B	←	giallo	C1-9
2	φ4	$\bar{B}$	←	arancio	C1-8
3	V+		←	rosso scuro	C1-7
4					
5	V+		←	rosso chiaro	C1-7
6	φ1	A	←	nero	C1-11
7	φ2	$\bar{A}$	←	marrone	C1-10
8					

Connettore P8b

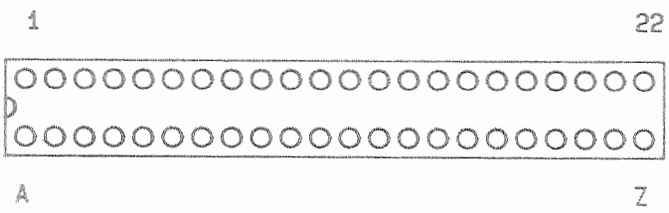


Piedini	Segnale	Note
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16	Start Convert	← B2-T
17	End of Conversion	→ B2-U
18		
19	+5V	
20	+15V	
21	-15V	
22	GND	

Connettore B1

Piedini	Segnale		Note	
A				
B	Data 7	MSB	→	P3-3
C	Data 6		→	P3-4
D	Data 5		→	P3-5
E	Data 4		→	P3-6
G	Data 3		→	P3-7
H	Data 2		→	P3-8
J	Data 1		→	P3-9
K	Data 0	LSB	→	P3-10
L				
M	Scorta			
N	Scorta			
P				
R	Analog In		←	P7-1
S	GND		←	P7-2
T				
U				
V				
W	+5V			
X	+15V			
Y	-15V			
Z	GND			

Connettore B1



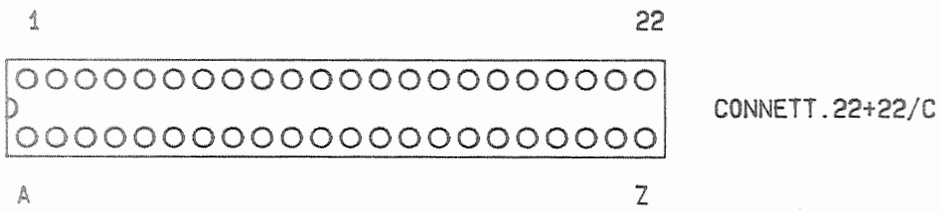
CONNETT.22+22/C

Piedini	Segnale	Note
1		
2		
3	DC	← P3-18
4	Moto	← P3-15
5	A/I	← P3-17
6	Lett	← P3-14
7		
8		
9		
10		
11	Start	← P2-1
12	Blank	← P2-2
13	Clock	← Z1-8
14		
15		
16		
17		
18		
19	+5V	
20	+15V	
21	-15V	
22	GND	

Connettore B2

Piedini	Segnale	Note
A		
B		
C		
D		
E		
G		
H	Passo	→ Z4-2
J	A/I	→ Z
K		
L	DF	→ P3-11
M		
N		
P		
R		
S		
T	Start C	→ B1-16
U	EOC	→ B1-17
V		
W	+5V	
X	+15V	
Y	-15V	
Z	GND	

Connettore B2

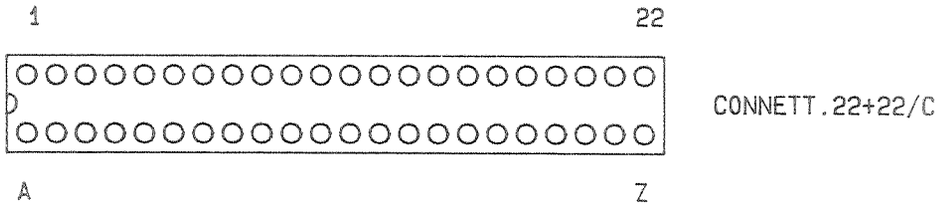


Piedini	Segnale	Note
1	GND	
2	GND	
3	GND	
4	GND	
5	GND	
6	GND	
7	GND	
8	GND	
9	GND	
10	GND	
11	GND	
12	GND	
13	GND	
14	GND	
15	GND	
16	GND	
17	GND	
18	GND	
19	GND	
20	GND	
21	GND	
22	GND	

Connettore B4

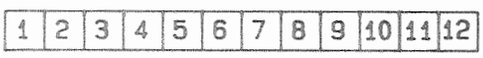
Piedini	Segnale	Note
A		
B	Start	→ P2a,1
C	Clock	→ P2a,3
D	Blank	→ P2a,2
E	+5V	← P2a,5-6
G		
H		
J		
K		
L		
M		
N	Video	→ P7-b
P		
R		
S		
T		
U		
V		
W		
X		
Y	-15V	← P2a,8
Z		

Connettore B4



Piedini	Segnale	Note		
1	GND			
2	+5V	←		
3	A/I	←	P4b-2	celeste
4	GND		P4b-3	bianco
5	Impulso moto	←	P4b-1	verde
6	+12V	←		
7	V+	→	P8b-3,5	rosso
8	φ4 $\bar{B}$	→	P8b-2	arancio
9	φ3 B	→	P8b-1	giallo
10	φ2 $\bar{A}$	→	P8b-7	marrone
11	φ1 A	→	P8b-6	nero
12	GND			

Connettore C1



Piedini	Segnale	Note
1	GND	P1-P7,8
2	+5V	→ P1-1,2
3	-15V	→ P1-5,6
4	GND	
5	+15V	→ P1-3,4

Connettore C3

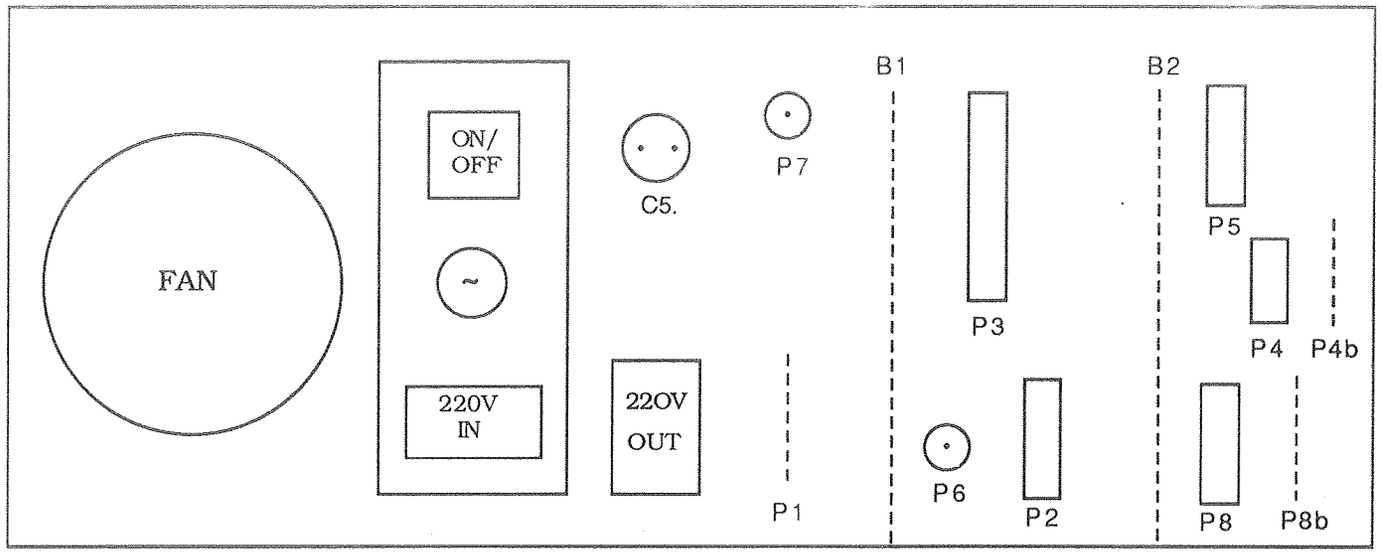
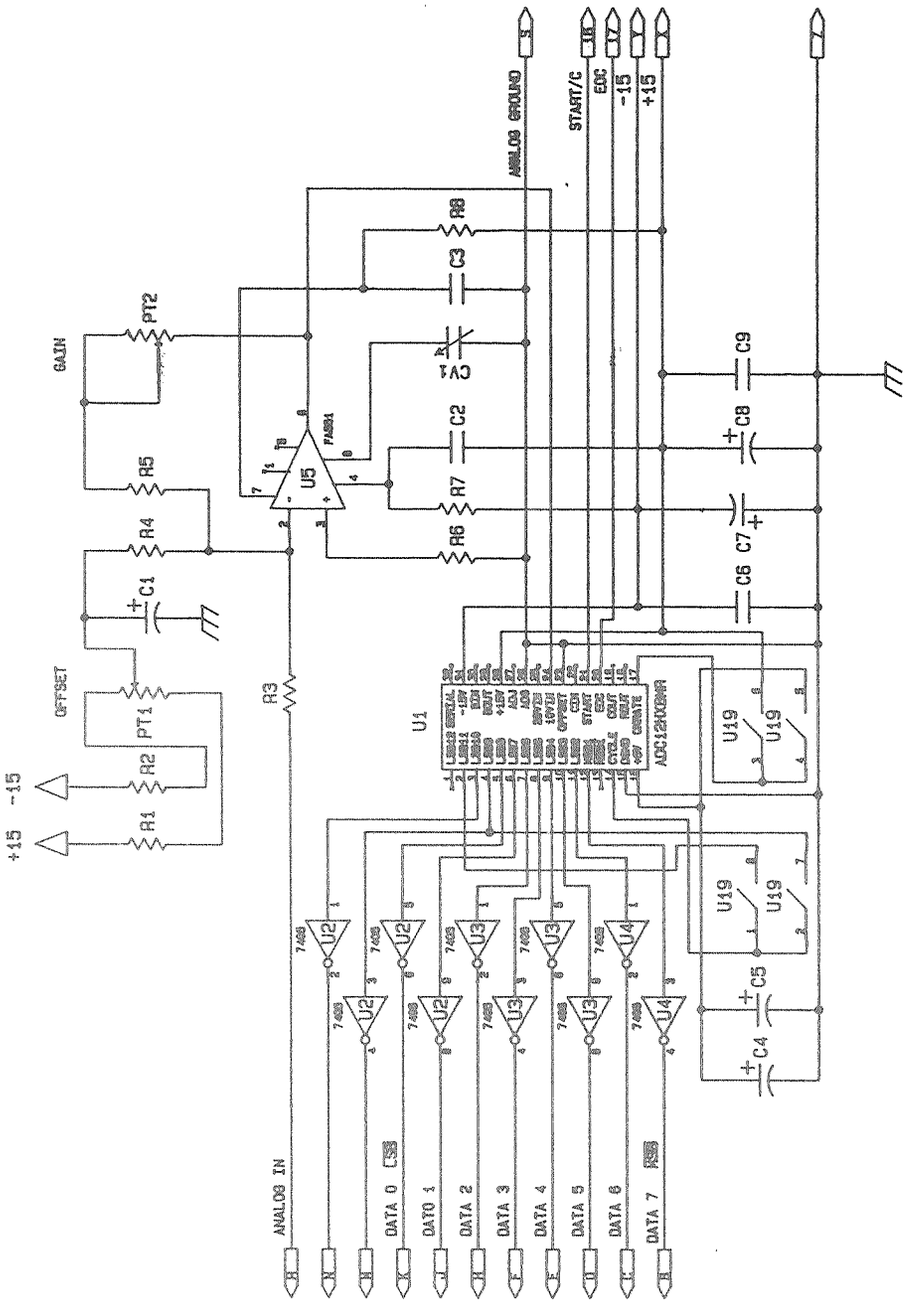


Fig. 2.2 - Vista posteriore del cassetto

3. *Schemi elettrici*

Nelle pagine seguenti sono riportati gli schemi elettrici delle schede a circuito stampato:

MFA B1:	Conversione A/D
MFA B2:	Controllo
MFA B3:	Master
MFA B4:	Indicatore di stato
MFA B5:	Adattatore
B4:	Scheda Reticon RC100B + RC108 per pilotaggio sensore.



DATA	DESCRIZIONE
7-3-90	MFA/B1
PROG.CAD	carlo A. Brotzu
REVISIONE	
FOGLIO... 1 di 4	

Figura 3.1 - Conversione A/D

U1 = ADC-HZ12B, A/D Converter
U2 = 7405, Hex inverter
U3 = 405, Hex inverter
U4 = 7405, Hex inverter
U5 = FA551, Op Amp
PT1 = potenziometro 10K per la regolazione dell'offset dell' amplificatore
PT2 = potenziometro 5K per la regolazione del guadagno dell' amplificatore
U19 = deviatore SW4A
TP1 = punto di prova per la misura del segnale di ingresso all'ADC.
CV1 = condensatore variabile 25 pF
R1 = 10K
R2 = 10K
R4 = 4.7K
R5 = 10K
R6 = 3.9K
R7 = 10 Ω
R8 = 10 Ω
C1 = 1μF
C2 = 100n
C3 = 100n
C4 = 1μF
C5 = 10μF
C6 = 10n
C7 = 1μF
C8 = 1μF
C9 = 10n

Per uscita su 8 bit sono collegati i piedini 14-4 e 17-28 di U1.

Lista componenti scheda MFA B1

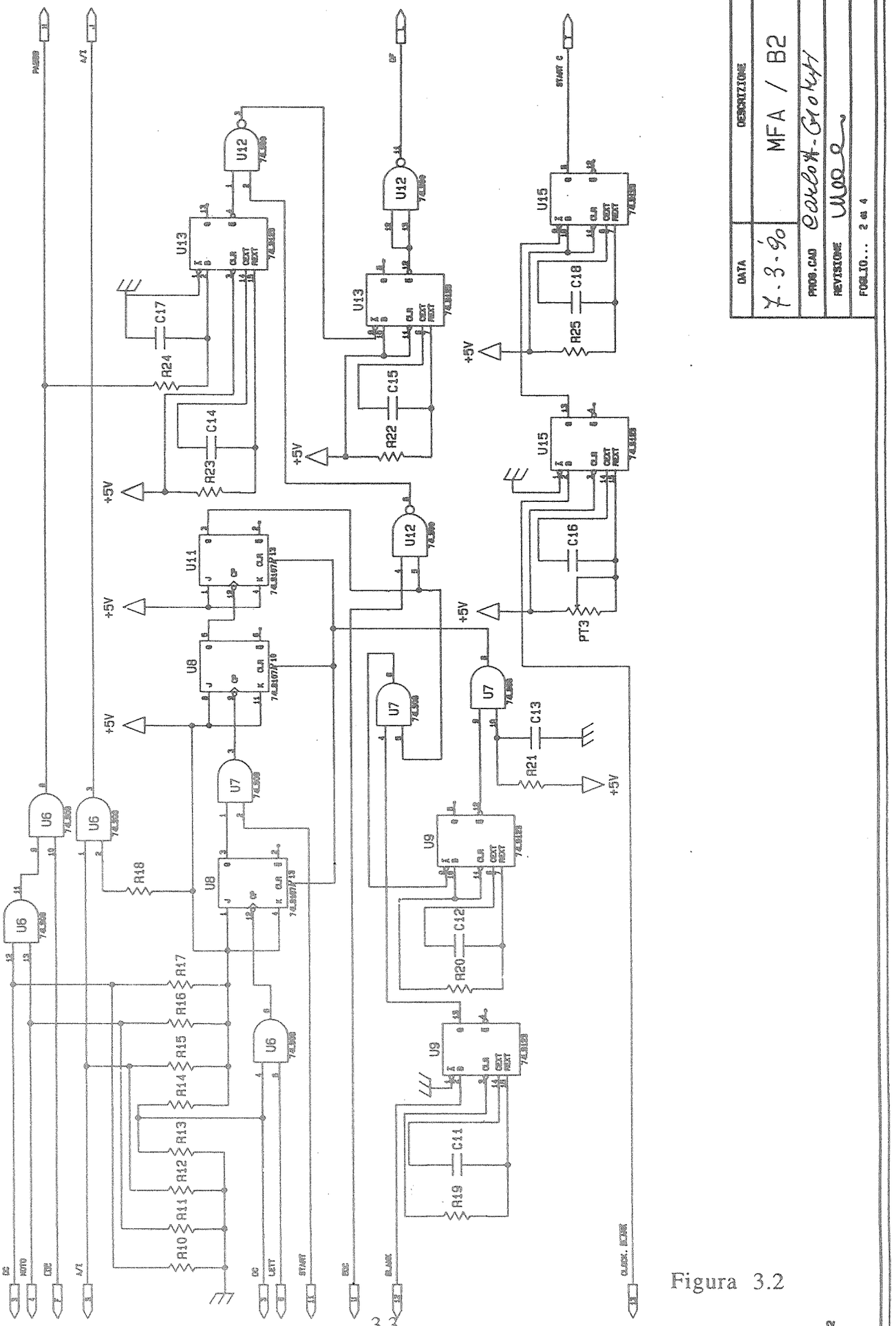

DESCRIZIONE
DATA
7-3-90
MFA / B2
PROG.CAD Eagle 3.0 Light
REVISIONE
FOGLIO... 2 di 4
+5V
U6
U7
U8
U9
U11
U12
U13
U15
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
PT3
C11
C12
C13
C14
C15
C16
C17
C18
START
CLOCK

Figura 3.2

U1 = 7408, Quad AND
U2 = 74107, Dual FF
U3 = 74107, Dual FF
U4 = 7408, Quad AND
U5 = 74123, Dual Univ
U6 = 7400, Quad AND
U7 = 74123, Dual Univ
U8 = 74123, Dual Univ

PT1 = 10K
R10 = 330 Ω
R11 = 330 Ω
R12 = 330 Ω
R13 = 330 Ω
R14 = 330 Ω
R15 = 330 Ω
R16 = 330 Ω
R17 = 330 Ω
R18 = 220 Ω
R19 = 8,2K
R20 = 8,2K
R21 = 1K
R22 = 8,2K
R23 = 33
R24 = 330
R25 = 8,2K
C11 = 560pF
C12 = 560pF
C13 = 1μF
C14 = 330n
C15 = 1n
C16 = 1.5μ
C17 = 220n
C18 = 560pF

Lista componenti scheda MFA B2

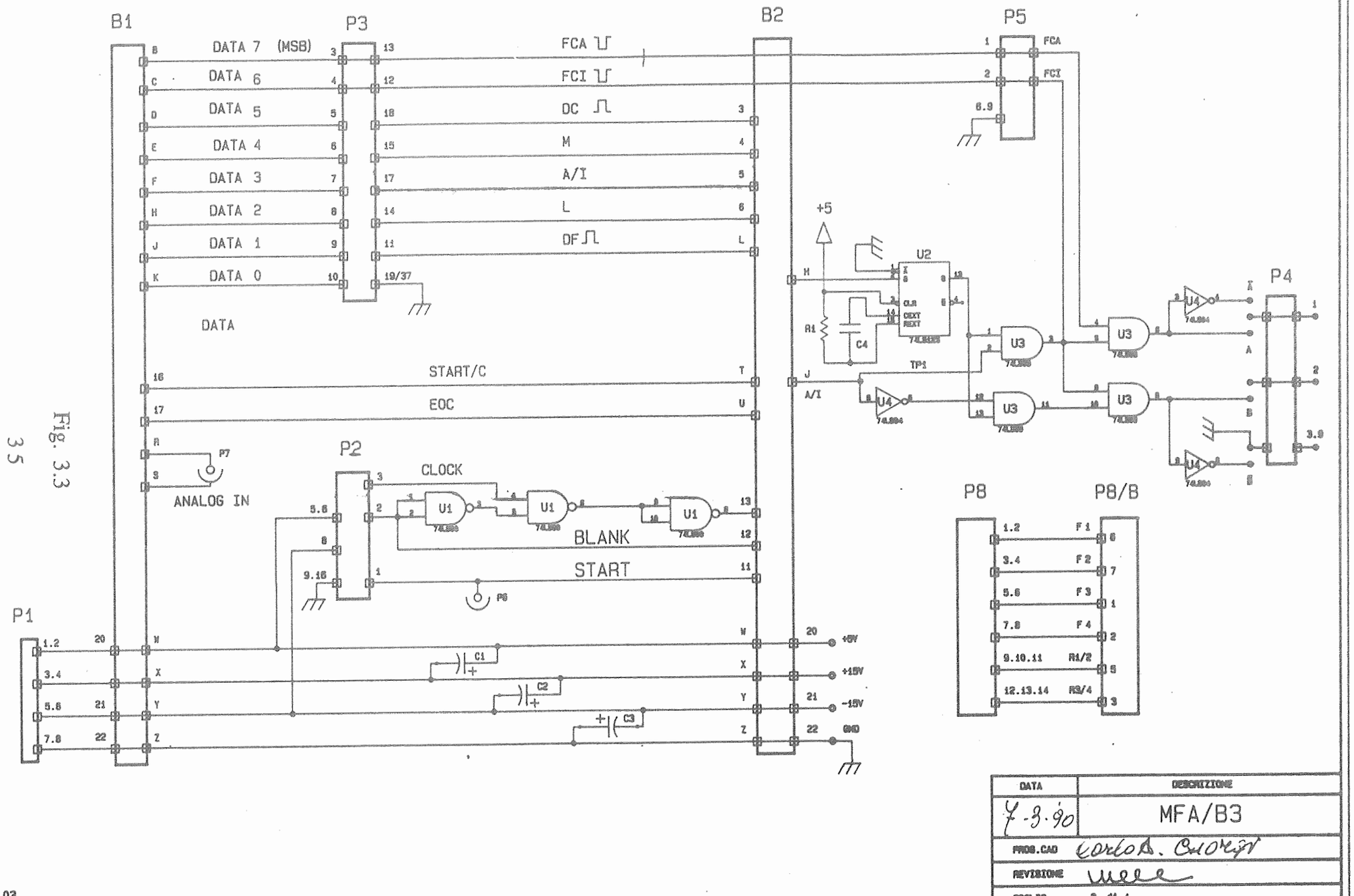


Fig. 3.3

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DATA	DESCRIZIONE
7-3-90	MFA/B3
PROG.CAD	Carlo A. Chiorri
REVISIONE	
FOGLIO...	3 di 4

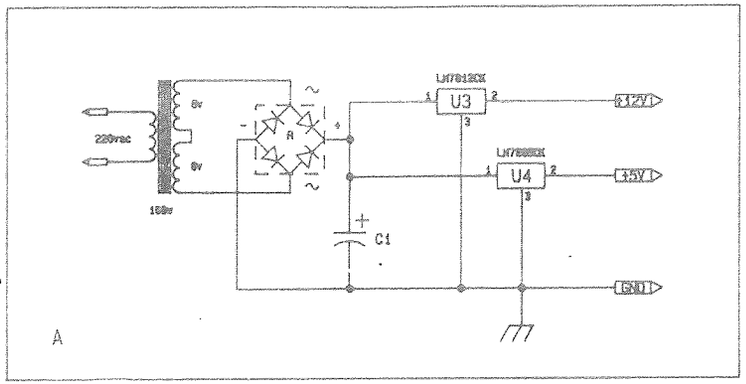
03

U1 = 7400, Quad AND
U2 = 74123, Dual Univ
U3 = 7408, Quad AND
U4 = 7432, Quad OR

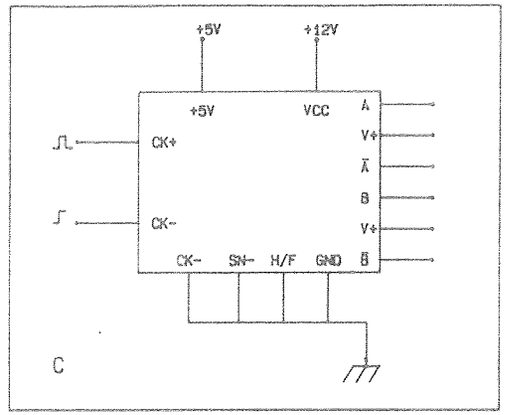
R1 = 10K

C1 = 10µF 25V
C2 = 10µF 25V
C3 = 10µF 25V
C4 =1n

Lista componenti scheda MFA B3



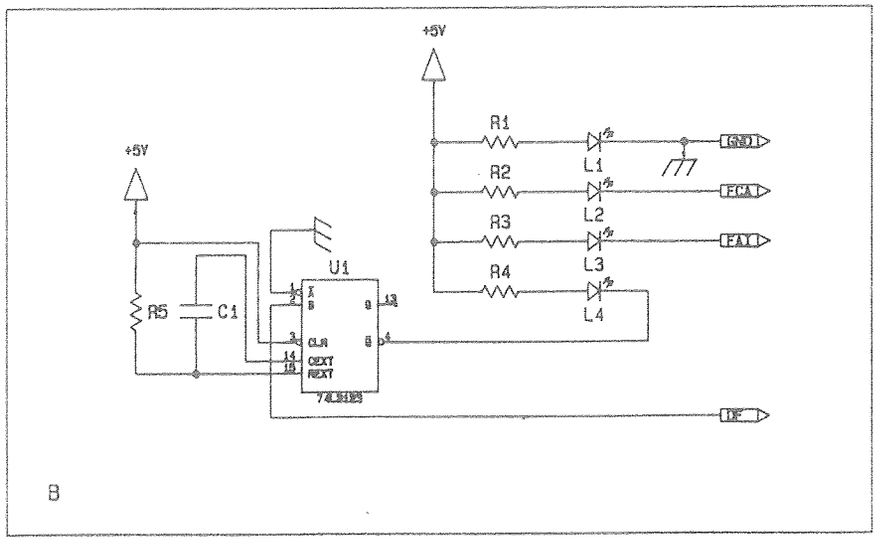
Alimentatori Motori Passo Passo



Attuatore P.P.

Fig. 3.4

37



Indicatori Di Stato

DATA	DESCRIZIONE
4-3-90	MFA/B4
PROG.CAD	Enrico M. Ghiotto
REVISIONE	
FOGLIO...	4 di 4

04

Alimentazione motori passo/passo

Trasformatore 220/6+6
Ponte R = 1A.40V.
Stabilizzatori U3 = LM7812CK U4 = 7805Ck
C1 = 640µF, 25V

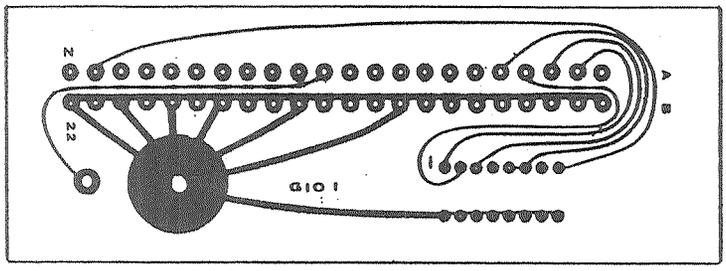
Indicatori di stato

U1 = 74LS1S2
R1 = 390Ω
R2 = 390Ω
R3 = 390Ω
R4 = 390Ω
R5 = 15KΩ
C1 = 22n
L1/L2/L3/L4/ LED.Ø 3 m/m

Lista componenti scheda MFA B4

MFA / B5

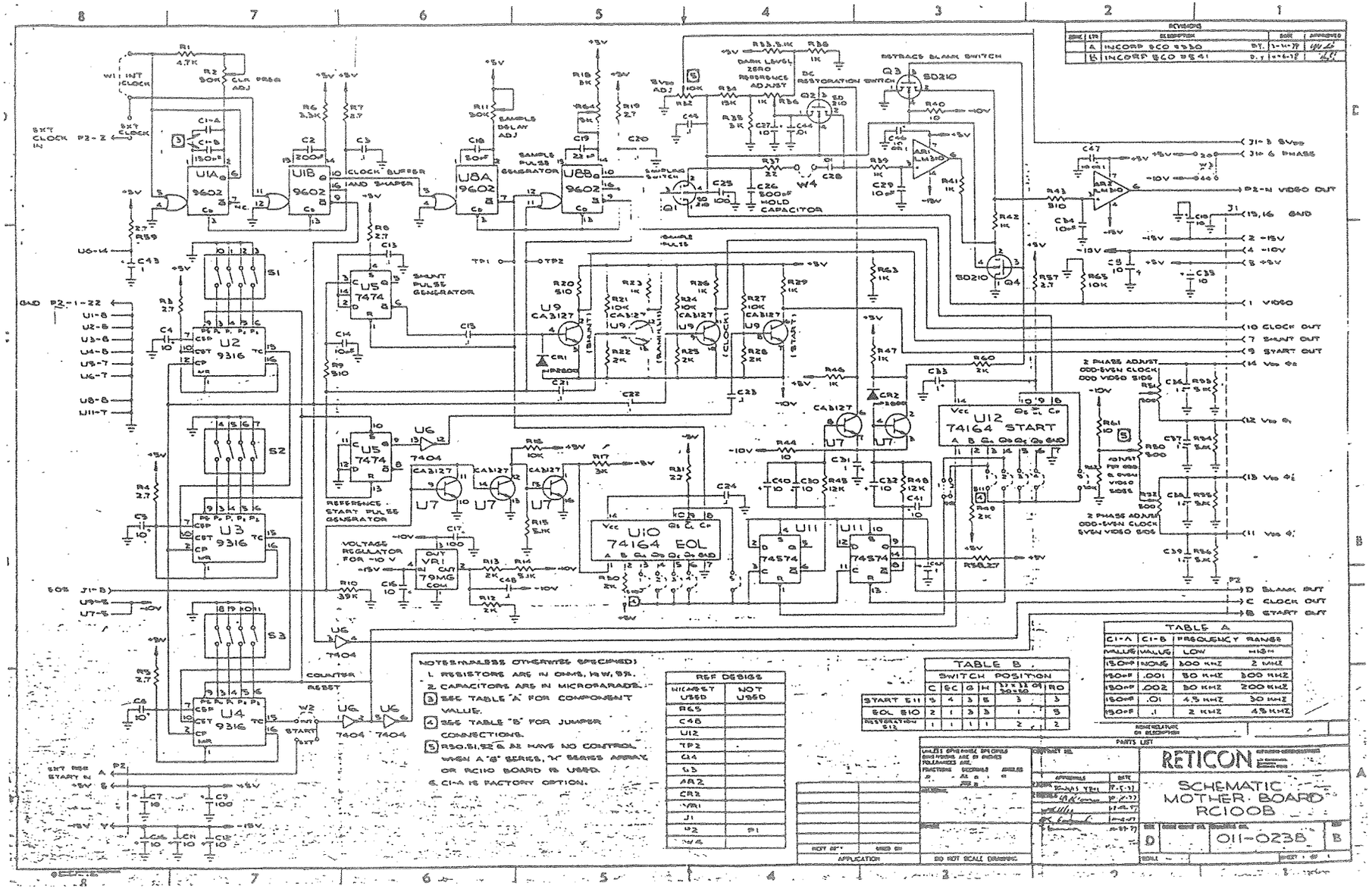
Basetta supporto connettore scheda RETICON RC-100B

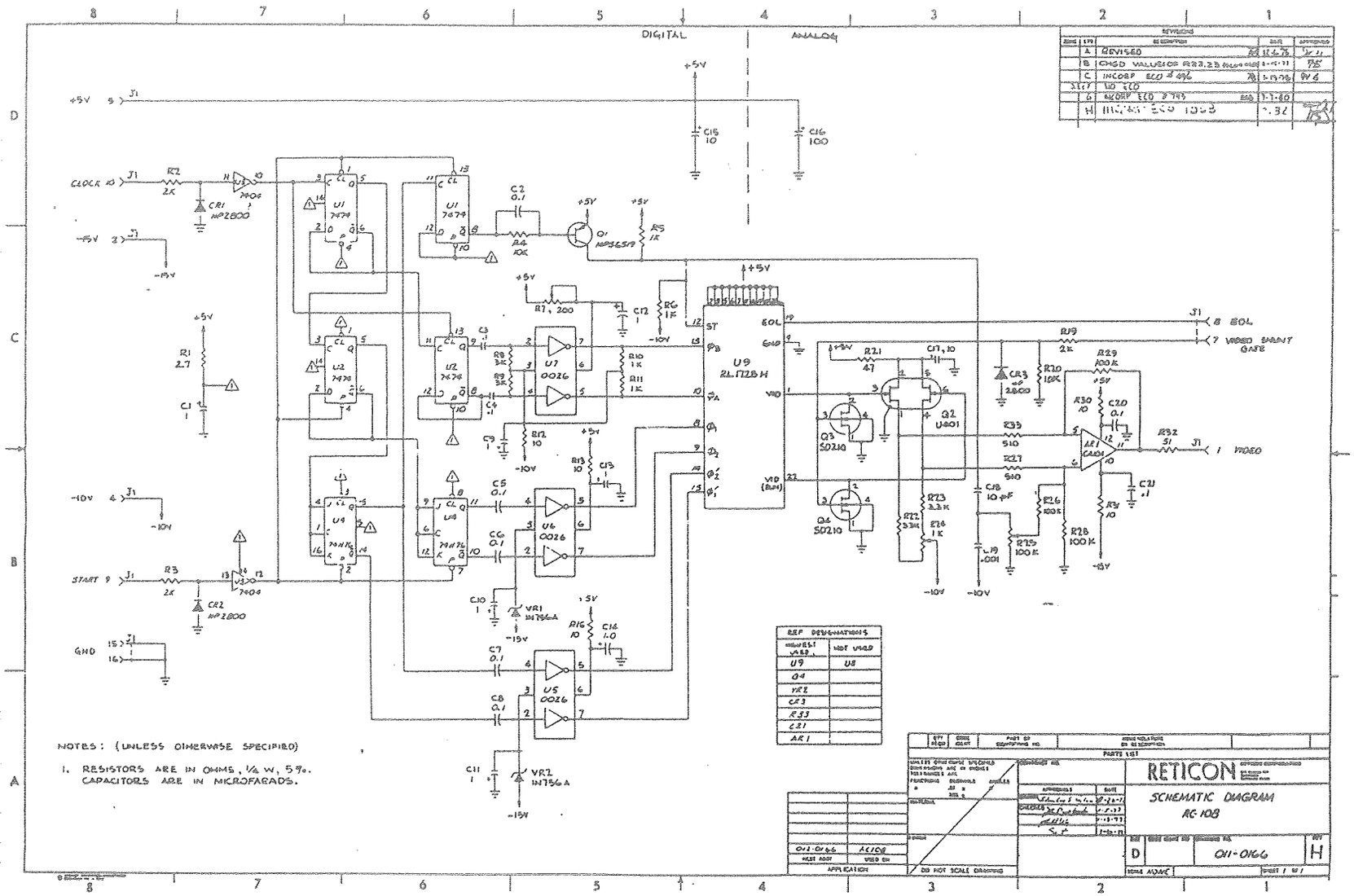


Piedini Connettore 22+22 Connettore 8+8

	B	Start Out ⎍ ⟶	1
	C	Clock Out ⎍ ⟶	3
	D	Blanking Out ⎍ ⟶	2
	E	+5v ⟵	5/6
	Y	-15v ⟵	8
da1a22		GND	da9a16
	N	Video Out ⟶	BNC

Fig. 3.5


REVISIONS
A INCORP ECO 9330
B INCORP ECO 9541
TABLE A
C1-A C1-B FREQUENCY RANGE
MYLAR MYLAR LOW HIGH
150PF 100PF 100 KHZ 2 MHZ
150PF .001 80 KHZ 300 KHZ
150PF .002 50 KHZ 200 KHZ
150PF .01 4.5 KHZ 30 KHZ
150PF .1 2 KHZ 45 KHZ
TABLE B
SWITCH POSITION
START S11
EOL S10
RESTORATION S13
NOTES UNLESS OTHERWISE SPECIFIED
1. RESISTORS ARE IN OHMS, 1/8W, 5%.
2. CAPACITORS ARE IN MICROFARADS.
3. SEE TABLE "A" FOR COMPONENT VALUE.
4. SEE TABLE "B" FOR JUMPER CONNECTIONS.
5. R50,51,52 & 53 HAVE NO CONTROL WHEN A "B" SERIES, "W" SERIES ARRAY OR RC110 BOARD IS USED.
6. C1-A IS FACTORY OPTION.
REF DESIGS
MICASET USED
NOT USED
PARTS LIST
RETICON
SCHEMATIC MOTHER BOARD RC100B
011-0238
DO NOT SCALE DRAWING


DIGITAL
ANALOG
+5V
-15V
-10V
CLOCK 10
START 9
GND
J1
U1 7474
U2 7474
U3 7404
U4 74H74
U5 0026
U6 0026
U7 0026
U9 2L1128H
Q1 MPS6519
Q2 U401
Q3 SD210
Q4 SD210
LE1 CA401
CR1 MP2800
CR2 MP2800
CR3 MP2800
VR1 IN756A
VR2 IN756A
R1 2.7
R2 2K
R3 2K
R4 10K
R5 1K
R6 1K
R7 200
R8 3K
R9 3K
R10 1K
R11 1K
R12 10
R13 10
R16 10
R19 2K
R21 47
R22 5.1K
R23 3.3K
R24 1K
R25 100K
R26 100K
R27 510
R28 100K
R29 100K
R30 10
R31 10
R32 51
R33 510
C1 1
C2 0.1
C3 1
C4 1
C5 0.1
C6 0.1
C7 0.1
C8 0.1
C9 1
C10 1
C11 1
C12 1
C13 1
C14 1.0
C16 10
C16 100
C17,10
C18 10 pF
C19 .001
C20 0.1
C21 .1
J1 8 EOL
J1 7 VIDEO SHUNT GATE
J1 1 VIDEO
REF DESIGNATIONS
U9 U8
Q4
VR2
CF3
R33
C21
AR1
NOTES: (UNLESS OTHERWISE SPECIFIED)
1. RESISTORS ARE IN OHMS, 1/4 W, 5%. CAPACITORS ARE IN MICROFARADS.
RETICON
SCHEMATIC DIAGRAM
RC-108
011-0166
H
DO NOT SCALE DRAWING

RC-108

4. Zoccolatura dei circuiti integrati

Nelle pagine seguenti sono riportate le zoccolature dei componenti integrati montati sulle schede MFA B1, MFA B2 e MFA B3.

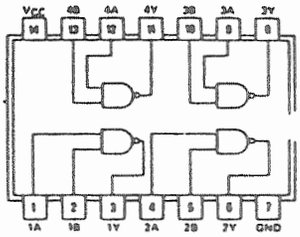
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

00

positive logic:
$Y = \overline{AB}$

See page 6-2



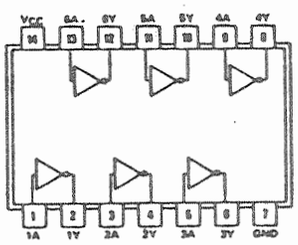
SN5400 (J) SN7400 (J, N)
SN54H00 (J) SN74H00 (J, N)
SN54L00 (J) SN74L00 (J, N)
SN54LS00 (J, W) SN74LS00 (J, N)
SN54S00 (J, W) SN74S00 (J, N)

HEX INVERTERS
WITH OPEN-COLLECTOR OUTPUTS

05

positive logic:
$Y = \overline{A}$

See page 6-4



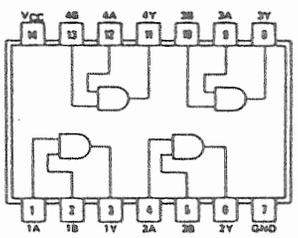
SN5405 (J) SN7405 (J, N)
SN54H05 (J) SN74H05 (J, N)
SN54LS05 (J, W) SN74LS05 (J, N)
SN54S05 (J, W) SN74S05 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-AND GATES

08

positive logic:
$Y = AB$

See page 6-10



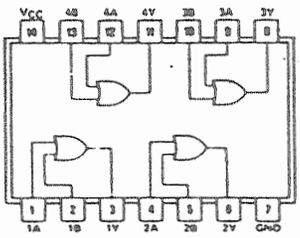
SN5408 (J, W) SN7408 (J, N)
SN54LS08 (J, W) SN74LS08 (J, N)
SN54S08 (J, W) SN74S08 (J, N)

QUADRUPLE 2-INPUT
POSITIVE-OR GATES

32

positive logic:
$Y = A+B$

See page 6-28



SN5432 (J, W) SN7432 (J, N)
SN54LS32 (J, W) SN74LS32 (J, N)
SN54S32 (J, W) SN74S32 (J, N)

DUAL J-K FLIP-FLOPS WITH CLEAR

107

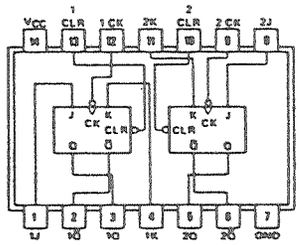
FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	

LS107A

FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$



SN54107 (J) SN74107 (J, N)
SN54LS107A(J) SN74LS107A(J, N)

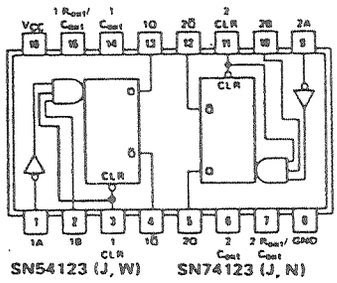
See pages 6-46 and 6-56

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

123

FUNCTION TABLE

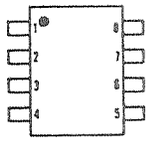
INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍



SN54123 (J, W) SN74123 (J, N)
SN54L123 (J) SN74L123 (J, N)
SN54LS123 (J, W) SN74LS123 (J, N)

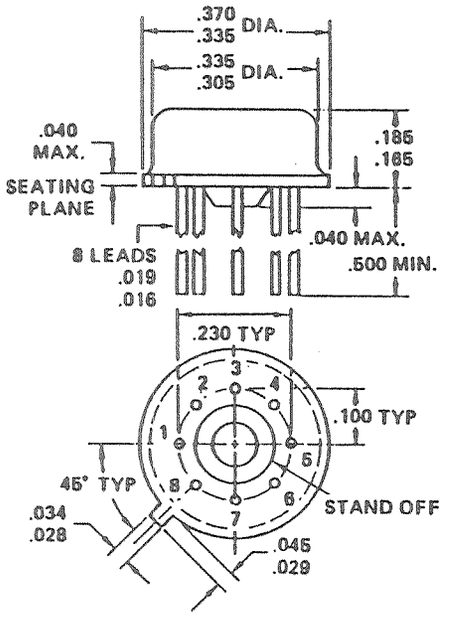
See page 6-76

DE and NB Dual In-line Packages
(Top View)



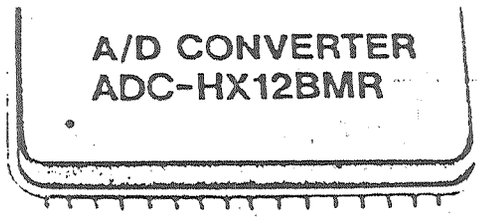
Order Part Nos.:
RC555NB, RV555NB
RC555DE, RV555DE, RM555DE

PIN	FUNCTION
1	GROUND
2	TRIGGER
3	OUTPUT
4	RESET
5	CONTROL VOLTAGE
6	THRESHOLD
7	DISCHARGE
8	V_{CC}

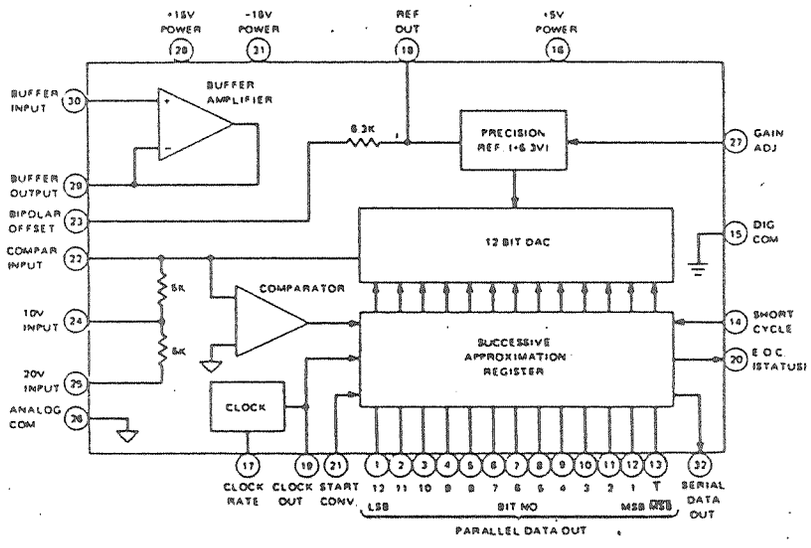


TO-99 CASE
FA550/51
A560/61
A570
CA580
FIGURE U

Pin	FA550/51 A560/61
1	Offset Adj.
2	IN –
3	IN +
4	–15V
5	Offset Adj.
6	OUT
7	+15V
8	Bandw. Cont.



(ACTUAL SIZE)



5. Operazioni di taratura

Nel caso di sostituzioni di componenti è necessario effettuare le operazioni di taratura indicate nella tabella I.

Regolazione		Scheda
1	Segnali i orologio del sensore	B4
2	Livello del segnale video	B4
3	Ritardo impulso di clock	MFA B2
4	Amplificazione segnale video	MFA B1

Tabella I - Sequenza delle operazioni di regolazione

5.1 Taratura della scheda sensore B4

Nelle pagine seguenti è riportata la procedura di taratura delle schede Reticon RC100 e RC108 (B4), che costituiscono i passi 1 e 2 del flusso di fig.4

La frequenza di clock viene regolata a 100 KHz.

RC-100B SERIES CIRCUIT BOARDS ALIGNMENT PROCEDURE

GENERAL DESCRIPTION
INTERNAL/EXTERNAL CLOCK OPERATION
INTERNAL/EXTERNAL START OPERATION

SECTION IV RC-100B MOTHERBOARD WITH RC-107 OR 108 AND "H" SERIES ARRAY

GENERAL DESCRIPTION

The Reticon RC-100B series circuit provides all clock, start, video amplifier, and blanking requirements for Reticon C, EC, G, H, and some RA series photodiode arrays.

Each circuit consists of two printed circuit boards -- an RC-100B "Motherboard", approximately 4.5 x 6 inches in dimension, which contains the clock and start generators, blanking circuit, sample-and-hold circuit, and buffer amplifiers, and the array board which contains a socket for the array, clock driver circuits, and a pre-amplifier.

Different array boards are needed for the various types of arrays:

RL-128C	--	RC-101	RL-128EC	--	RC-101
RL-256C	--	RC-101	RL-256EC	--	RC-102
RL-512C	--	RC-102	RL-512EC	--	RC-103
RL-768C	--	RC-103	RL-384EC	--	RC-103
RL-1024G	--	RC-103			
RL-128G	--	RC-104	RL-1024H	--	RC-107
RL-256G	--	RC-104	RL-1728H	--	RC-108
RL-512G	--	RC-105	RA-50x50A	--	RC110-01
RL-1024G	--	RC-106	RA-32x32A	--	RC110-02

The array boards are connected to the RC-100B Motherboard via connector J1/P1, or an optional 16-pin, 30 inch maximum, flat ribbon cable can be used. J1 is the 16-pin connector located approximately in the center of the RC-100B board. P1 is the male mating connector located on the array board. P2 is the edge connector of the RC-100B board.

INTERNAL/EXTERNAL CLOCK OPERATION

The RC-100B Motherboard contains an internal clock generator which supplies the master timing signal. Provisions are also made for an external clock input.

For internal clock operation, jumper INT CLOCK. The frequency range of the internal clock is controlled by the selection of capacitors C1-A and C1-B. Refer to Table A of Drawing Number 011-0238 for values for desired frequency range. R2, a 50K pot will allow for variance of the frequency within the selected frequency range. Boards are shipped from the factory with the clock frequency set at approximately 500KHz internal operation

For external clock operation, jumper EXT CLOCK, and apply an external clock into P2-Z. The external clock pulse should be an active TTL high clock with a minimum pulse width of 20ns, and a maximum pulse width of 200 μs.

INTERNAL/EXTERNAL START OPERATION

The RC-100B Motherboard contains an internal start pulse generator. Provisions for an external start pulse are also available.

For internal start operation, jumper INT START and set the desired interval between the start pulses, using the three four-position rocker switches S1, S2, and S3. Each switch has a weight of 2^n and a maximum count of 4096 is available. For optimum operation, the scan time should not exceed 40ms, because dark current increases with longer integration time. The minimum count between start pulses is eight, plus the number of elements in the array. Boards are shipped from the factory set in this configuration.

NOTE

If a scan time of >5 ms is used, change C28 on the RC-100B board to a .1μf capacitor.

Because of an inherent count of one in the start pulse generator, the setting on the rocker switches will be one less than the actual count, i.e., if a count of 520 is desired, set the rocker switches to 519.

The blanking period (time between last element of previous scan and first element of next scan) is defined as the count of the start pulse generator minus the number of elements in the array.

For external start operation, jumper EXT START and inject an external start signal into P2-A. The external start should be an active high TTL pulse with a minimum pulse width of the clock pulse width plus 50ns, and a maximum pulse width of less than one clock period.

If an external start is used, it should be synchronized with the negative-going edge of the clock to insure that the start pulse envelopes one and only one positive transition of the clock pulse.

POWER REQUIREMENTS

Connect +5 volts @ 700ma and -15 volts @ 300ma to P2-E and P2-Y, respectively. Connect ground to any pin from P2-1 to P2-22.

SECTION IV

ALIGNMENT PROCEDURE

RC-100B MOTHERBOARD WITH RC-107 OR 108 AND "H" SERIES ARRAY

1. Jumper Connections. Split pads are provided to program the RC-100B board for the desired configuration. Refer to Table B of Drawing Number 011-0238 for correct configuration. See Figure 1 for location of split pads.

2. Monitor TP1 and adjust R2 (if internal clock is used) for the desired frequency. The maximum frequency is 1.5MHz. Adjust R11 for a 200ns, negative going pulse width.

3. Monitor P2-B and set the desired start pulse interval (if internal start is used). Synchronize the oscilloscope at P2-B during alignment.

4. Monitor TP2 and adjust R64 for a 100ns pulse width.

5. Monitor J1-I. With the array in dark, adjust R24, (1K pot on the array board) to zero the base line of the video. Saturate the array and readjust R24, if necessary, so no signal or switching spikes go more negative than -8V dc. Do not over saturate.

NOTE

R51, R52, R50, and R32 on the RC-100B board will have no effect when an "H" series array board is used.

6. With the array still in dark, adjust R7 (200 Ω pot on the array board) for best odd/even pattern.

7. Monitor the video output at P2-N. With the array in dark, adjust R36 on the Motherboard until the video is centered with the blanking level.

8. Adjust R25 (100K pot on the array board) until the first three video elements are as close in amplitude as possible to the other elements.

9. Adjust R11 until optimum performance is derived on the video. Optimum adjustment of R11 resulting in a balance of maximum video output, minimum switching spikes, and a fixed pattern tracking from dark to 90% of saturation. This adjustment will interact with the previous adjustments. Go back to Step 5 and touch up as necessary.

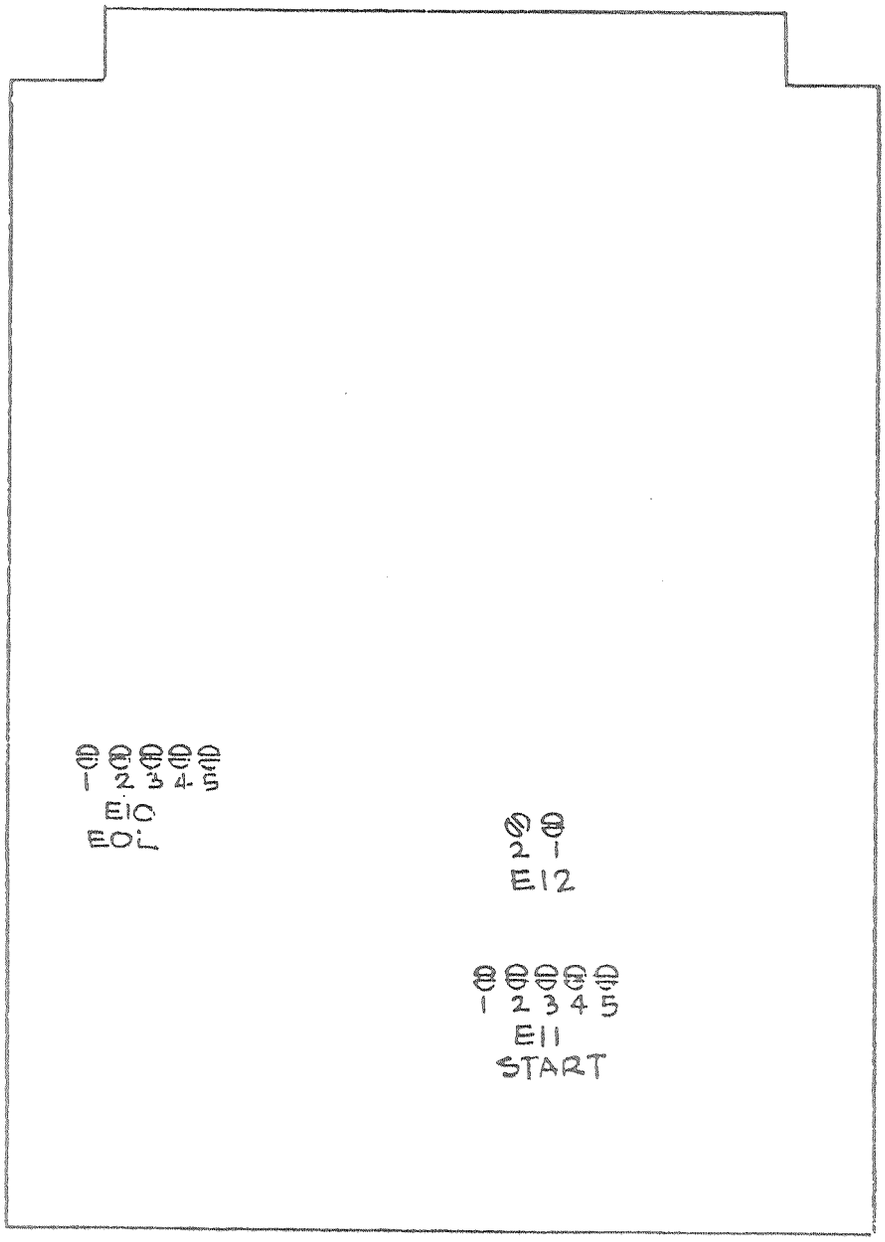
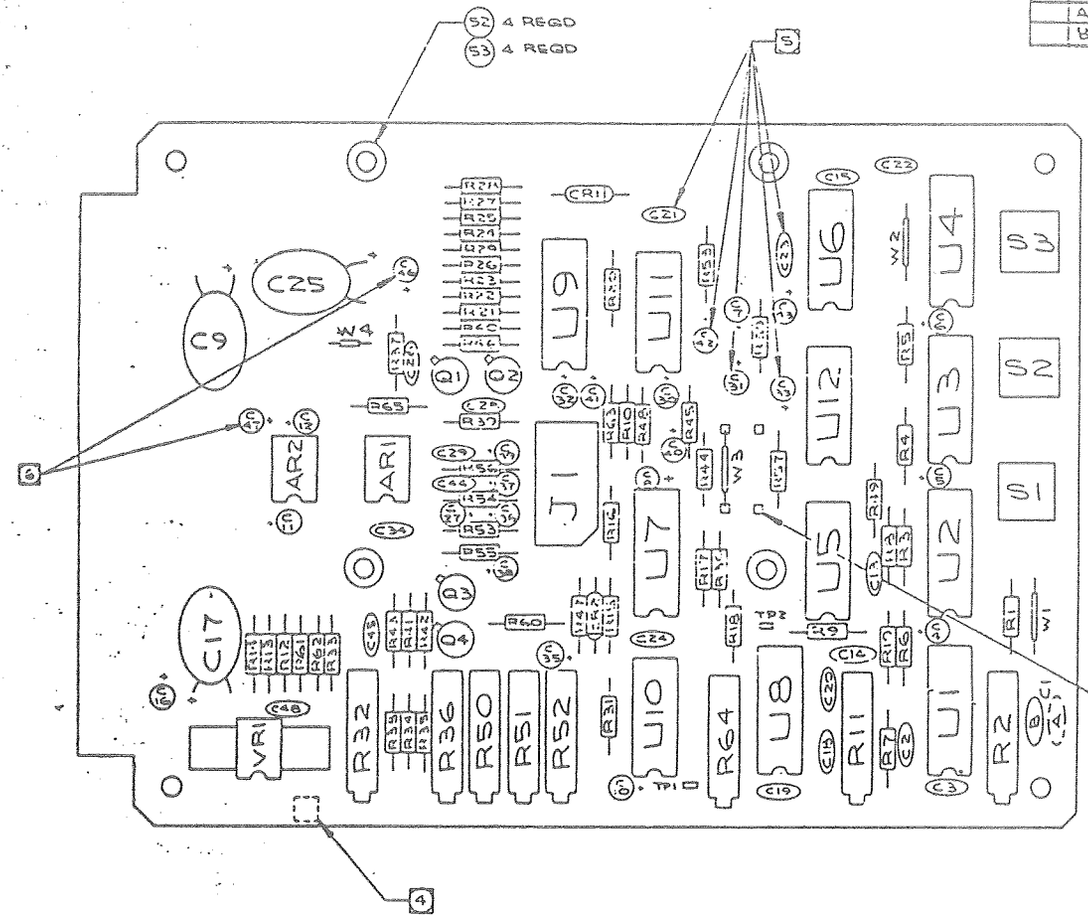


Figure 1 Split Pad Location

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	INCORP ECO #530 DY.	1-11-78	
	B	INCORP ECO #541 DY.	4-6-78	



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. COMPONENT HEIGHT WITHIN STANDOFFS IS .56 ± .3 MAX. REMAINING COMPONENTS MAY BE .50 MAX.
2. LEAD PROTRUSION SHALL BE .09 MAX.
3. FOR SCHEMATIC SEE DWG 011-0238
4. INKSTAMP ASSY REV LETTER IN LOCATION SHOWN USING BLACK INK. COVER WITH ONE COAT OF CLEAR KRYLON #1303.
5. LAY C21, 23, 31, 33 & 42 DOWN BEFORE SOLDERING.
6. C46, 47 ARE FACTORY SELECT.
7. MASK HOLES FOR C1-A, EXT START AND CLOCK PRIOR TO DIP SOLDERING.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL SEE P/L

FINISH

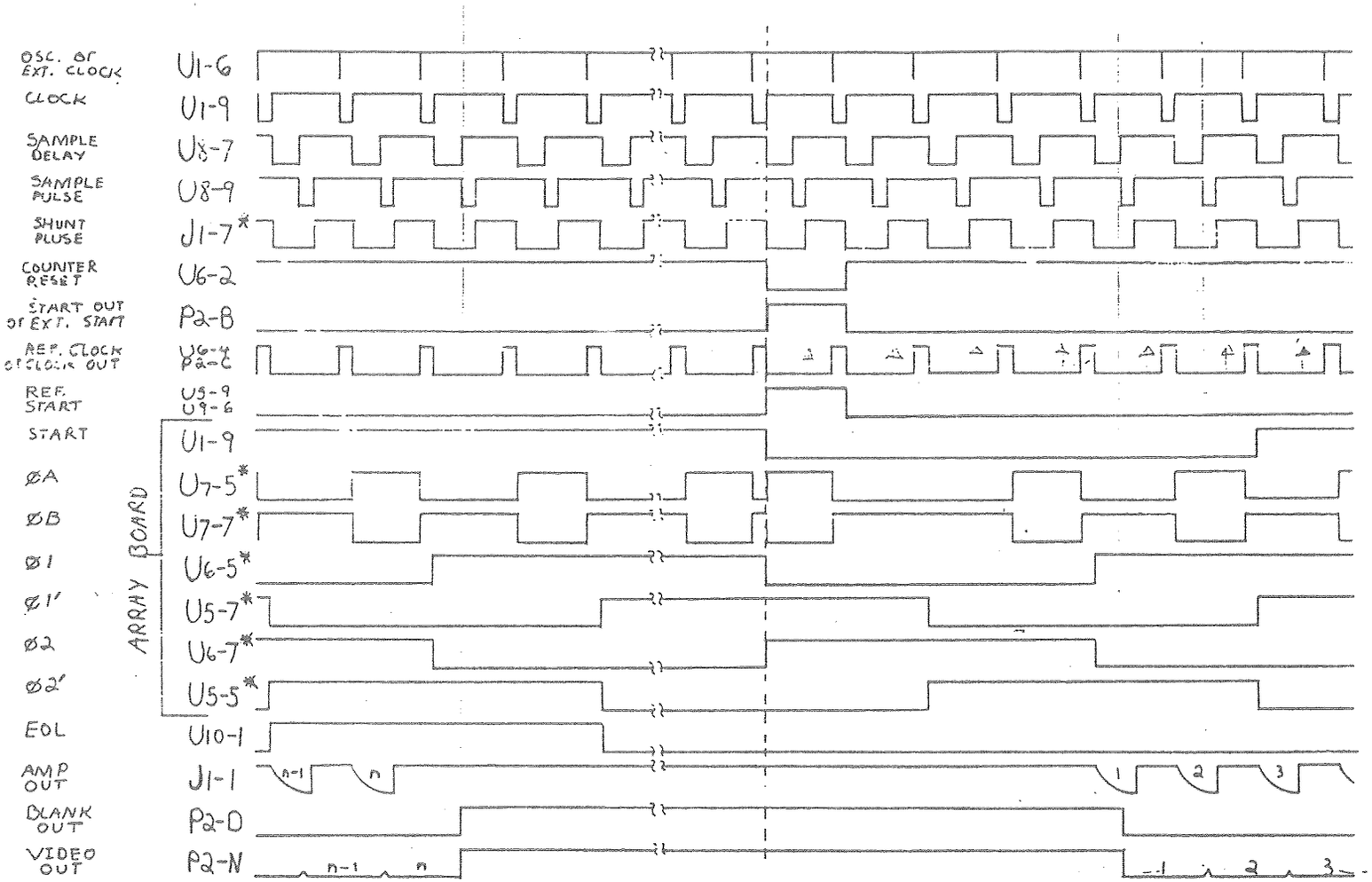
CONTRACT NO.

APPROVALS	DATE
DRAWN [illegible]	9-2-77
CHECKED [illegible]	9-7-77
[illegible]	9-12-77
[illegible]	9-26-77
T. [illegible]	11-14-77

RETICON
RETICON CORPORATION
an [illegible] company

ASSEMBLY, P.C. BOARD MOTHER BOARD RC100B

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C		010-0238	B



* Denotes MOS Level Signals. ALL Other Except Video Are TTL

Timing Diagram
RC-100B Series Circuit Boards
H Series Array

5.2 Taratura della scheda MFA B2

Il segnale di clock del sensore, generato dalla scheda MFA B4 viene inviato sul piedino 13 della scheda MFA B2, ritardato e rigenerato mediante la coppia di univibratori U8 e inviato tramite il piedino T della scheda all'ingresso Start Conversion del convertitore A/D. Per regolare il ritardo si deve:

1) collegare i piedini 13 e T agli ingressi di un oscilloscopio a doppia traccia, sincronizzato sul piedino 13 (clock)
2) ruotare il trimmer collegato ai piedino 3-15 di U8 per ottenere in T un impulso ritardato di 2-3 μs rispetto all'impulso di clock.

5.3 Taratura della scheda MFA B1

Il convertitore A/D è predisposto per un range d'ingresso tra 0V e 10V, mediante il collegamento fra i piedini 23 e 26 di U1; il segnale video prodotto dalla scheda B4 viene riportato tra questi estremi agendo sui potenziometri PT1 e PT2.

Per regolare il segnale si deve:

1) collegare l'ingresso dell'amplificatore U5 (piedino R della spina) e l'uscita (TP1) ad un oscilloscopio a doppia traccia, sincronizzato sull'impulso di start generato da B4 e prelevabile dal BNC start situato sulla parte posteriore del cassetto portaelettronica
2) oscurare il sensore e regolare PT1 (Offset) per avere 0V in TP1
3) portare il sensore in saturazione e regolare PT2 per avere 10V in TP1.

Ripetere i punti 2) e 3) fino a raggiungere la migliore condizione.

6. *Caratteristiche*

Nelle pagine seguenti sono riportate le caratteristiche dei moduli e componenti:

RL1024/RL2048 Reticon	(trasduttore optoelettronico)
RC 555 Raytheon	(multivibratore)
FA551 Intronics	(operazionale)
ADC-HZ Datel	(convertitore A/D)
89903001 Crouzet	(motore p-p)

EG&G RETICON

H-SERIES SOLID STATE LINE SCANNERS
1024, 1728 AND 2048 ELEMENTS A7

The Reticon H-Series devices are high resolution solid state image sensors designed specifically for facsimile and related applications. These monolithic silicon integrated circuits contain a row of 1024, 1728 or 2048 photodiodes on 15 μm centers, together with shift register scanning circuits for sequential readout. The RL-1728H and 2048H allow high-resolution facsimile using only a single device to read a full 8.5-inch page width. The RL-1024H may be used for lower resolution requirements. Key features of these components are:

- **High resolution — up to 2048 sensors on 15 μm centers.**
- **Internal scanning for serial video output.**
- **Differential output to eliminate fixed-pattern noise.**
- **Charge storage mode operation for high sensitivity.**
- **Simple external circuitry using standard components.**
- **Standard dual in-line package with optical window.**

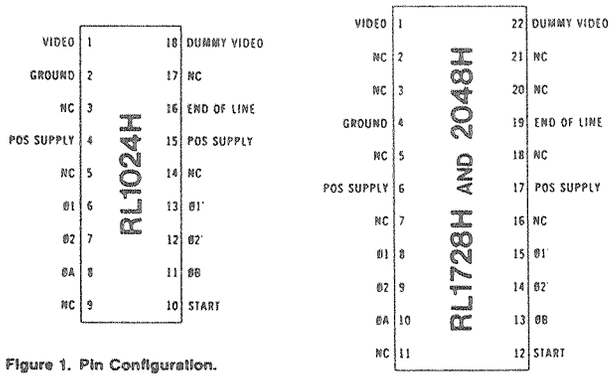


Figure 1. Pin Configuration.

GENERAL DESCRIPTION

The Reticon "H" series is a family of monolithic self-scanning linear photodiode arrays. The devices in this series consist of a row of silicon photodiodes, each with an associated storage capacitor on which to integrate photocurrent and a multiplex switch for periodic readout via an integrated shift register scanning circuit. The part number of each device indicates the number of elements in the array (e.g., 1024 or 1728). "H" series devices have sensors on 15μm (0.59 mil) centers. The sensing area is defined by an aperture which is 16μm wide and runs the full length of the array.

The devices are packaged in 18 or 22 lead dual-in-line integrated circuit packages with ground and polished optical windows. Pin configurations for the "H" devices are shown in Fig. 1.

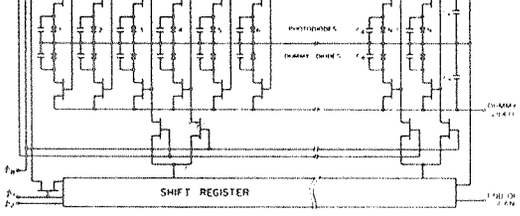


Figure 2. Equivalent circuit.

EQUIVALENT CIRCUIT

A simplified equivalent circuit of an "H" series line scanner is shown in Fig. 2. Each cell consists of a photosensor and a parallel storage capacitor, and is connected through an MOS transistor switch to a common video output line. The switches are turned on and off in sequence by the shift register multiplexing circuits, thereby periodically recharging each cell to 5 volts and storing approximately 1.8 pcoul on its capacitance. The multiplexing circuits are driven by six clock phases which are easily generated from a TTL master clock which sets the cell-to-cell sampling rate. During the line scan time, the charge on each capacitor is gradually removed by the reverse current flowing in the associated photodiode.

The reverse current is made up of two components: the photocurrent—and the dark leakage current (which is typically less than 0.5pA at room temperature and can be neglected). The photocurrent is proportional to the light intensity or irradiance. During a line scan time, the charge removed from each cell is the product of the photocurrent and the line time. This charge must be replaced through the video line when the diode is sampled once each scan. Thus, the output signal obtained from each scan of an N element array is a train of N charge pulses each proportional to the light intensity on the corresponding photodiode.

The "H" series devices also contain a row of dark dummy diodes which are in one-to-one correspondence with the sensing diodes. By sampling the sensing diodes and the dark diodes differentially, switching transients associated with the multiplex switches are eliminated. This gives a high quality video signal with a minimum of external circuitry.

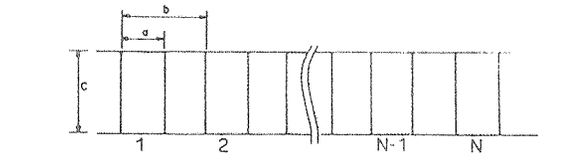


Figure 3. Sensor geometry and idealized aperture response function.

SENSOR GEOMETRY

In the "H" series line scanners the light sensing area is a long, narrow rectangular region defined by an aperture in an opaque mask. Bar-shaped photodiodes extend across the aperture and are connected to the storage capacitors and multiplex switches which are buried under the mask. The entire aperture is photosensitive; photocurrent generated by light incident between the photodiodes will be collected by the nearest diode. Figure 3 shows the aperture geometry and an idealized response function which would be obtained by scanning a point source of visible light along the length of the aperture.

The dimensions a, b, and c indicated in Fig. 3 are as follows: the photodiode width *a* is 7μm, the photodiode spacing *b* is 15 μm and the aperture width *c* is 16 μm. Wide aperture H-Series devices with dimension *c* = 300 μm are available in 1024 and 2048 elements. They are the RL1024H/20 and RL2048H/20 respectively.

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EG&G RETICON H-SERIES SOLID STATE LINE SCANNERS 1024, 1728 AND 2048 ELEMENTS

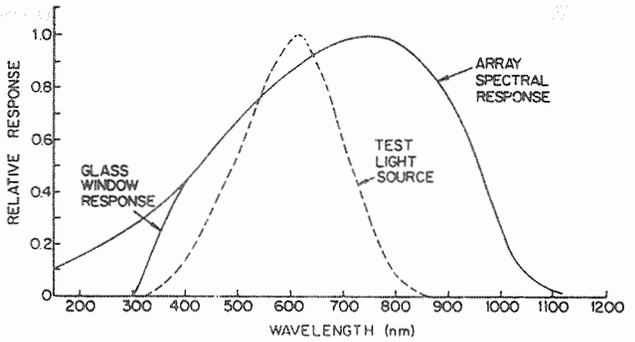


Figure 4. Relative spectral response as a function of wavelength. Dotted line shows spectral distribution of light source used for sensitivity measurements. Quartz and glass windows have similar response except the glass window will fall off at approximately 300 nm as shown above.

SENSITIVITY AND SPECTRAL RESPONSE

The spectral response of the H-series devices is similar to that of other high quality silicon photodetectors, covering the range from the near UV to the near IR. A glass window is standard for arrays with a 16 μm aperture while arrays with the 300 μm aperture have a quartz window. Relative spectral response is shown as a function of wavelength in Fig. 4. Note that relatively high responsivity is maintained even in the blue end of the spectrum because there is no interfering structure covering the diode. As most facsimile related applications for these devices use visible light, sensitivity and uniformity of response are specified using a source with the spectral distribution shown in the dotted line of Fig. 4. This special distribution is produced by filtering a 2870° K tungsten source with a Fish-Schurman HA-11 heat absorbing filter, 1 mm thick.

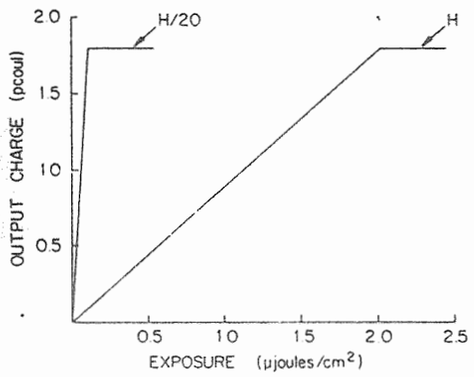


Figure 5. Signal charge per cell as a function of exposure for light source of Figure 4.

Since Reticon line scanners operate in the charge storage mode, the charge output of each diode (below saturation) is proportional to exposure, i.e. the irradiance or light intensity multiplied by the integration time or the time interval between successive start pulses. Thus there is an obvious trade-off between scanning speed and the required light intensity. Plots of charge output versus exposure are shown in Figure 5 for the light source of Figure 4 and the amplifier circuit of Figure 8.

Uniformity of response along the length of a photodiode array is also a function of wavelength. Devices tend to be less uniform at long wavelengths (IR) and more uniform at short wavelengths (visible). The non-uniformity specifications of the H-series are based on the light source of Fig. 4.

DARK RESPONSE AND DYNAMIC RANGE

There are three components to the dark output signal from a Reticon "H" series line scanner.—(1) the integrated dark leakage current—(2) the fixed pattern caused by incomplete cancellation of clock switching transients between the sensing and dummy diodes—and (3) the random pixel noise.

The dark leakage current will vary significantly from element to element but is typically less than 0.5 pA per diode at room temperature. Assuming this value, leakage current would contribute a saturation output charge of 1.8 pcoul with a 4 second line time. Thus, dark current will contribute about 1% of the saturated output signal for t_L=40 msec, 0.1% for t_L=4 msec, and so on. The dark current is a very strong function of temperature, approximately doubling every 7° C. Thus the maximum allowable line time becomes correspondingly shorter at high temperatures and longer at low temperatures. An important feature of these devices is the low power dissipation, which means that self-heating is negligible.

The switching transients are very nearly cancelled by the differential output. Residual uncancelled transients will result in a fixed pattern which is less than 0.5% of the saturated output signal for unprocessed video.

Pixel noise is the random, non-repetitive fluctuations which are superimposed on the dark level, and is the ultimate limiting noise which cannot be removed by signal processing. Its rms value will generally be amplifier limited at a value less than about 0.1% of the saturation level, depending on the noise bandwidth and preamplifier used.

The dynamic range that can be achieved is circuit dependent. Care must be exercised in circuit layout to provide for adequate ground plane, circuit decoupling, and avoidance of electrostatic pickup. The typical dynamic range for the RL1728H array operating in the RC1728H/LN low noise evaluation circuit is 375:1 when measured as a ratio of the saturation output to the peak to peak dark fixed pattern. The typical dynamic range is 3000:1 when the saturation level is compared to the rms noise on each pixel.

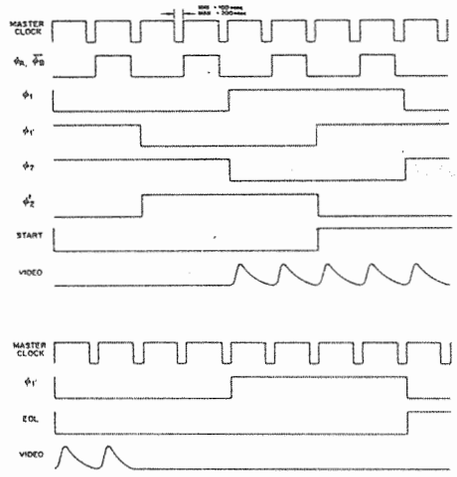


Figure 6. Timing Diagram for "H" Series Devices.

DRIVE REQUIREMENTS

Six clock phases are required to drive the "H" series devices and a properly timed start pulse is required to initiate each scan. Figure 6 shows the proper timing of the input clock and start signals. Note that $\emptyset_1$ and $\emptyset_2$, and $\emptyset'_1$ and $\emptyset'_2$ are two pairs of complementary square waves. The $\emptyset_A$ and $\emptyset_B$ clocks are complements, but are not square waves. Diodes are sampled on the negative going transitions of $\emptyset_1$, $\emptyset_B$, $\emptyset'_1$, $\emptyset_B$, $\emptyset_2$, $\emptyset_B$, $\emptyset'_2$, $\emptyset_B$, $\emptyset_1$,. The start pulse timing is non-critical except that it must be negative for one positive going transition of $\emptyset_1$ and the following positive going transition of $\emptyset'_1$. The number of master clock periods n between start pulses is arbitrary except that it must be equal to or greater than

N where N is the number of sensors in the array.

A suitable drive circuit for the "H" series devices is shown in Figure 7. The start count n may be set at any value up to 4096 by closing the appropriate set of switches on the 9316 counters.

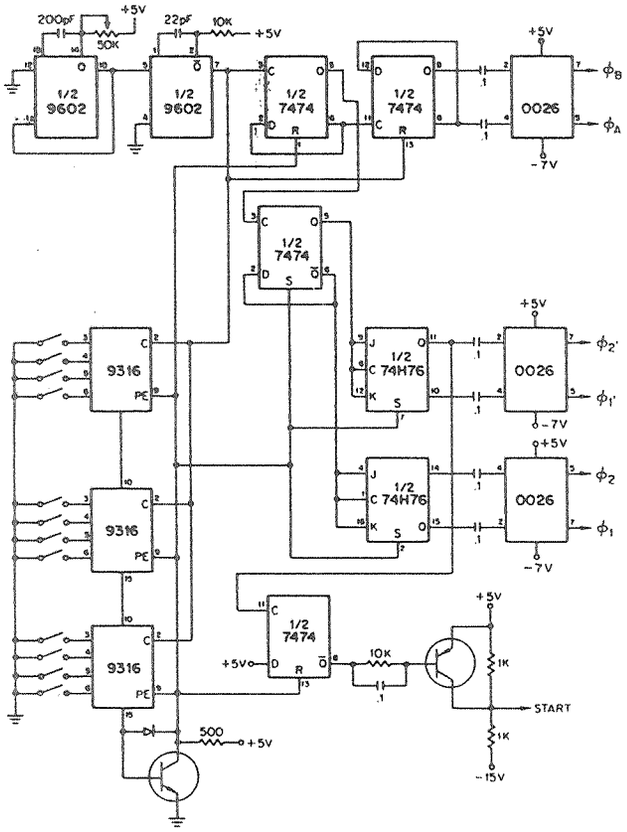


Figure 7. Drive Circuit for "H" Series Devices.

SIGNAL EXTRACTION

The video output of the "H" series devices is a train of N charge pulses flowing onto the video line capacitance during each scan with timing as shown in Figure 6. Superimposed on the video signal are periodic switching transients which are introduced by the multiplex circuitry. Since these same transients also appear without the signal on the dummy video line, the two outputs may be amplified differentially to obtain a clean video signal. Two types of amplifier circuits are in common use. These are: (1) a simple differential current amplifier; and (2) a video line integration, sample-and-hold circuit. The former has a pulse output while the latter has a boxcar output with greater signal to noise ratio.

CURRENT AMPLIFIER. A simple amplifier circuit using the Reticon CA-10A op amp connected as a differential amplifier is shown in Fig. 8. An example of the video output of this circuit is shown in the oscilloscope photographs of Fig. 9.

INTEGRATE, SAMPLE AND HOLD AMPLIFIER. alternative signal processing scheme, the output charge pulses are integrated on the video and dummy line capacitances. The voltage change on these output lines is then amplified differentially, and sampled-and-held for one master clock period. After sampling, the output lines are reset to integrate the next charge pulse. The result is a sampled and held boxcar video signal such as that shown in Fig. 10.

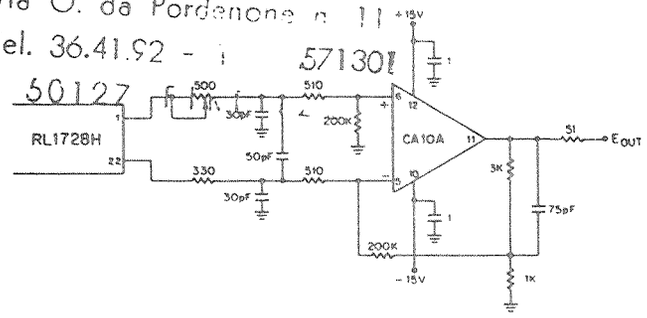


Figure 8. Suggested Amplifier Circuit.

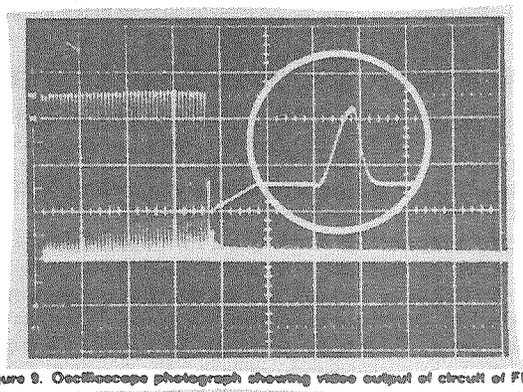


Figure 9. Oscilloscope photograph showing video output of circuit of Figure 8.

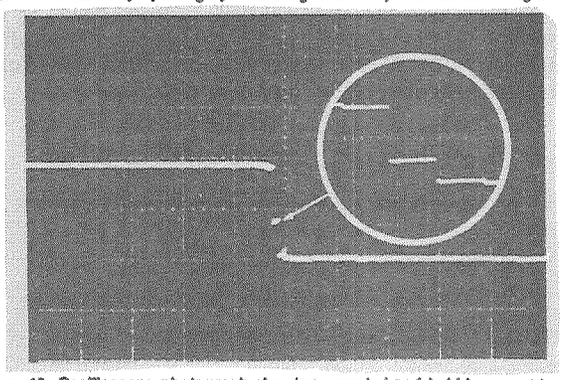


Figure 10. Oscilloscope photograph showing sampled and held boxcar video signal.

END-OF-SCAN OUTPUT

An end-of-scan output pulse is provided when the last two diodes are sampled. This end-of-scan output is provided primarily for test purposes and if not in use it should be shorted externally to the +5 volt supply. In those cases where the end of scan pulse is used, the voltage excursion of the end-of-scan pin should be minimized by using a circuit such as that shown in Fig.11. The timing of the end-of-scan output is shown in Fig. 6.

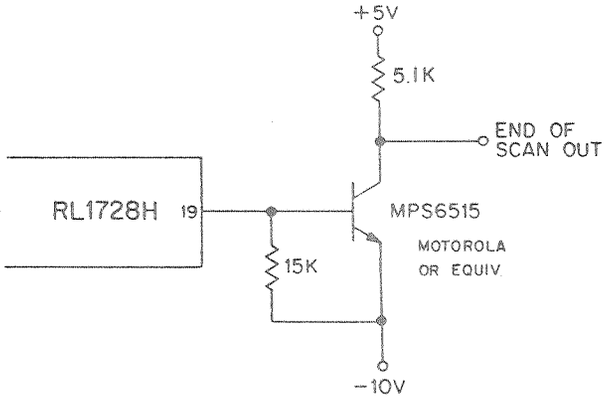


Figure 11. Suggested end of scan output circuit.

CIRCUIT CARDS

Printed circuit cards containing all required drive and amplifier circuitry for operation of the "H" series self-scanning photodiode arrays are available from Reticon. These circuits are highly recommended for the first time array evaluation. In many cases they are also useful for design into final equipment.

Three families of circuit cards are available. These circuits are complete except for power supplies and have the flexibility to operate over a wide range of scan rates and integration times.

RC1024H and RC1728H. These boards incorporate the drive circuit of Fig. 7 and the amplifier circuit of Fig. 8. They provide a pulse type output such as that shown in Fig. 9 and give good performance at lowest cost. The boards are 4 x 4.75 inches and have mounting holes in each corner. An example is shown in the photograph of Fig. 12. The RC1728H circuit can be used with the RL2048H as well as the RL1728H array.

RC100B SERIES. These circuits provide an integrated, sampled and held boxcar output such as that shown in Fig. 10. They are recommended for high performance applications which require this output waveform. Each circuit is divided into two boards—a standard "motherboard" which contains most of the circuitry and a small "array board" which connects to the motherboard via a ribbon cable and contains only those components which must be located close to the array. The motherboard (RC100B) is 4.5 x 6.5 inches in size and is terminated by a standard 22 pin edge connector. The array boards are 3 x 3.625 inches and have mounting holes in each corner. An RC107 array board is required for the RL1024H and an RC108 board for the RL1728H or RL2048H.

RC1728H/LN. This low noise circuit board is now available for the 1728 and 2048H series arrays. This low cost circuit is simple to operate and provides a sample and held video output with a typical P-P dynamic range of 375:1.

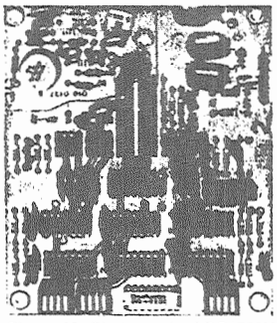


Figure 12. Photograph of RC1728H circuit board with RL1728H array.

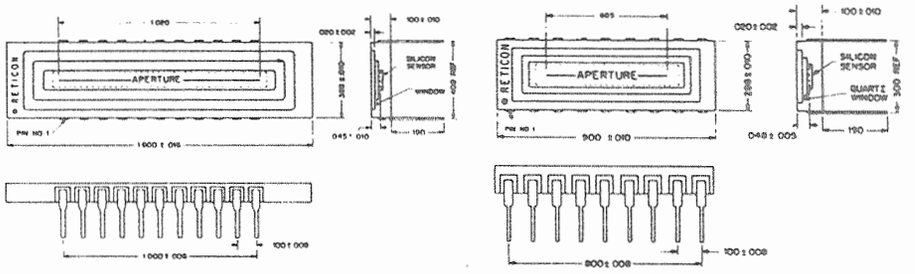


Figure 13. Outline drawing of RL-1728H (left) and RL-1024H (right). The RL2048H is similar to the RL1728H except the aperture length is 1.209 and the overall package length is 1.8 rather than 1.6.

ELECTRICAL CHARACTERISTICS (25° C)

	Min.	Typ.	Max.	Units
[1]Positive Supply Voltage V_P	4.5	5	5.5	volts
Clock Voltage High V_{CH}	V_P - 1	5	V_P	volts
Clock Voltage Low V_{CL}	-7.5	-7	-6.5	volts
Start Voltage High V_{SH}	V_P - 1	5	V_P	volts
Start Voltage Low V_{SL}	-7.5	-7	-5	volts
Sample Frequency f_s			3	MHz
[2]Clock Input Capacitance (Phases 1, 1', 2, 2')				
RL-2048H		60		pF
RL-1728H		50		pF
RL-1024H		30		pF
[2]Clock Input Capacitance (Phases A, B)				
RL-2048H		130		pF
RL-1728H		105		pF
RL-1024H		65		pF
[2]Video Line Capacitance Cv				
RL-2048H		60		pF
RL-1728H		50		pF
RL-1024H		30		pF
End-of-Scan Output Resistance		5		K ohms

ELECTRO-OPTICAL CHARACTERISTICS (25° C)

	Typ.	Units
Number of Sensors		
RL1024H, H/20	1024	
RL1728H	1728	
RL2048H, H/20	2048	
Center-to-center Spacing	15	μm
Aperture Length		
RL1024H, H/20	1.536	cm
RL1728H	2.592	cm
RL2048H, H/20	3.072	cm
Aperture Width		
H	16	μm
H/20	300	μm
[3]Sensitivity		
H	0.9	pA/μwatt/cm²
H/20	17	pA/μwatt/cm²
[4,6]Non-Uniformity of Sensitivity		
H, H/20	10	±%
[3]Saturation Exposure		
H	2.0	μjoules/cm²
H/20	.1	μjoules/cm²
Saturation Charge		
H, H/20	1.8	pcoul
[5]Dynamic Range		
H, H/20	375	

ABSOLUTE MAXIMUM RATINGS

	Min.	Max.	Units
Voltage on Any Terminal	V_P -20	V_P	volts
Storage Temperature	-55	+125	°C
Temperature Under Bias	-55	+85	°C

NOTES:
1. No terminal should ever be allowed to go more positive than V_P.
2. Capacitance measured at 5 volts bias.
3. Specified for light source of Fig. 4.
4. Specified for the light source of Fig. 4 neglecting first 4 and last 4 diodes.
5. RL1728H measured in RC1728H/LN circuit board at 1 MHz scan rate neglecting first 4 and last 4 diodes. Dynamic range is defined as the ratio of saturation signal to peak fixed pattern noise in the dark.
6. Maximum non-uniformity of sensitivity is ±15%.

GENERAL DESCRIPTION

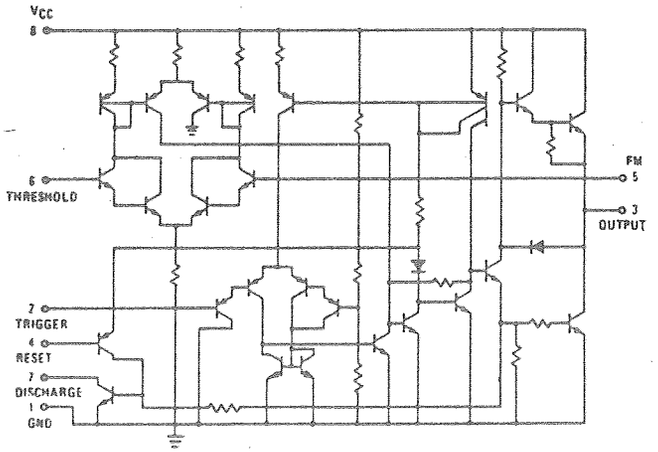
The RC555 and RM555 monolithic timing circuits are highly stable controllers capable of producing accurate time delays or oscillation. In the time delay mode, delay time is precisely controlled by only two external parts: a resistor and a capacitor. For operation as an oscillator, both the free running frequency and the duty cycle are accurately controlled by two external resistors and a capacitor.

Terminals are provided for triggering and resetting. The circuit will trigger and reset on falling waveforms. The output can source or sink up to 200mA or drive TTL circuits.

DESIGN FEATURES

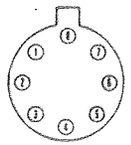
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- Output Drives TTL
- High Current Output Can Source or Sink 200mA
- Temperature Stability of 0.005%/°C
- Normally On and Normally Off Output

SCHEMATIC DIAGRAM



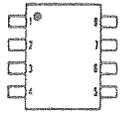
CONNECTION INFORMATION

TE Metal Can Package
(Top View)



Order Part Nos.:
RC555T, RM555T

DE and NB Dual In-line Packages
(Top View)



Order Part Nos.:
RC555NB, RV555NB
RC555DE, RV555DE, RM555DE

PIN	FUNCTION
1	GROUND
2	TRIGGER
3	OUTPUT
4	RESET
5	CONTROL VOLTAGE
6	THRESHOLD
7	DISCHARGE
8	V_{CC}

ABSOLUTE MAXIMUM RATINGS

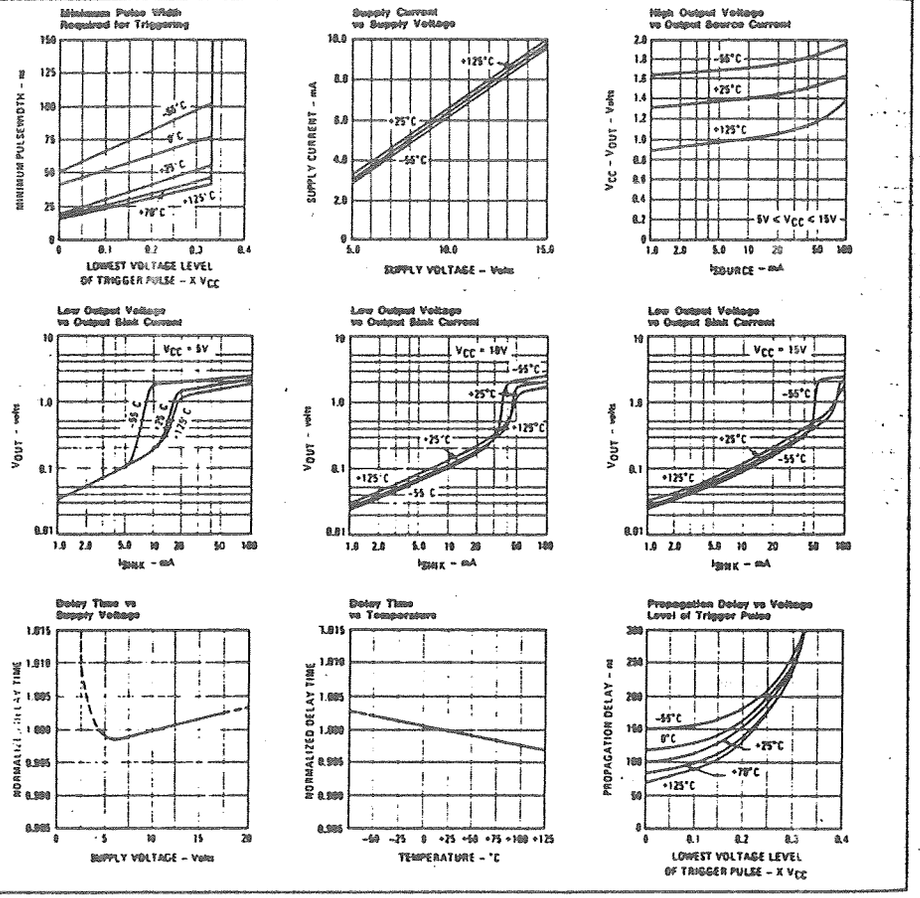
Supply Voltage	+18V	Operating Temperature Range	
Power Dissipation	600mW	RC555	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	RV555	−40°C to +85°C
Lead Temperature (Soldering, 60s)	+300°C	RM555	−55°C to +125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V to +15V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	RM555			RV/RC555			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞		10	12		10	15	mA
	Low State, (Note 1)							
Timing Error	R_A, R_B = 1kΩ to 100kΩ							
	C = 0.1μF (Note 2)							
Initial Accuracy			0.5	2		1		%
Drift with Temperature			30	100		50.1		ppm/°C
Drift with Supply Voltage			0.05	0.2		0.1		%/Volt
Threshold Voltage			2/3			2/3		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current	(Note 3)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage Drop (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100mA		2	2.2		2	2.5	V
	I_{SINK} = 200mA		2.5			2.5		
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.25				V
	I_{SINK} = 5mA					0.25	0.35	
Output Voltage Drop (high)	I_{SOURCE} = 200mA							
	V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100mA							
	V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

NOTES:
1. Supply current when output high typically 1mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V.
3. This will determine the maximum value of R_A + R_B. For 15V operation, the max total R = 20 megohm.

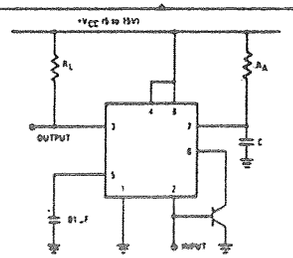
TYPICAL ELECTRICAL DATA



TYPICAL APPLICATIONS

Missing Pulse Detector

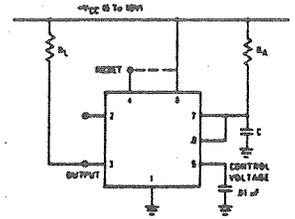
With the RC555/RM555 connected as shown, the timing cycle will be continuously reset by the input pulse train. A change in frequency, or a missing pulse, allows the timing cycle to go to completion and change the output level. For proper operation the time delay should be set slightly longer than the normal time between pulses.



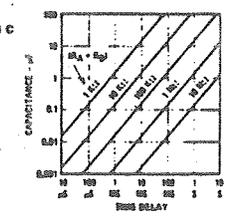
TYPICAL APPLICATIONS (Cont.)

Monostable Operation

In this mode, the timer functions as a one-shot. The external capacitor is initially held discharged by a transistor internal to the timer. Applying a negative trigger pulse to Pin 2 sets the flip-flop, driving the output high and releasing the short-circuit across the external capacitor. The voltage across the capacitor increases with time constant $\tau = R_A C$ to 2/3 V_{CC}, where the comparator resets the flip-flop and discharges the external capacitor. The output is now in the low state.

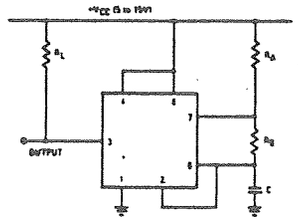


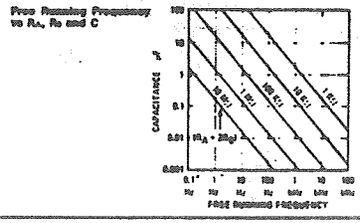
Circuit triggering takes place when the negative-going trigger pulse reaches $1/3V_{CC}$ and the circuit stays in the output high state until the set time elapses. The time the output remains in the high state is $1.1R_AC$ and can be determined by the graph. A negative pulse applied to Pin 4 (reset) during the timing cycle will discharge the external capacitor and start the cycle over again beginning on the positive-going edge of the reset pulse. If reset function is not used, Pin 4 should be connected to V_{CC} to avoid false resetting.



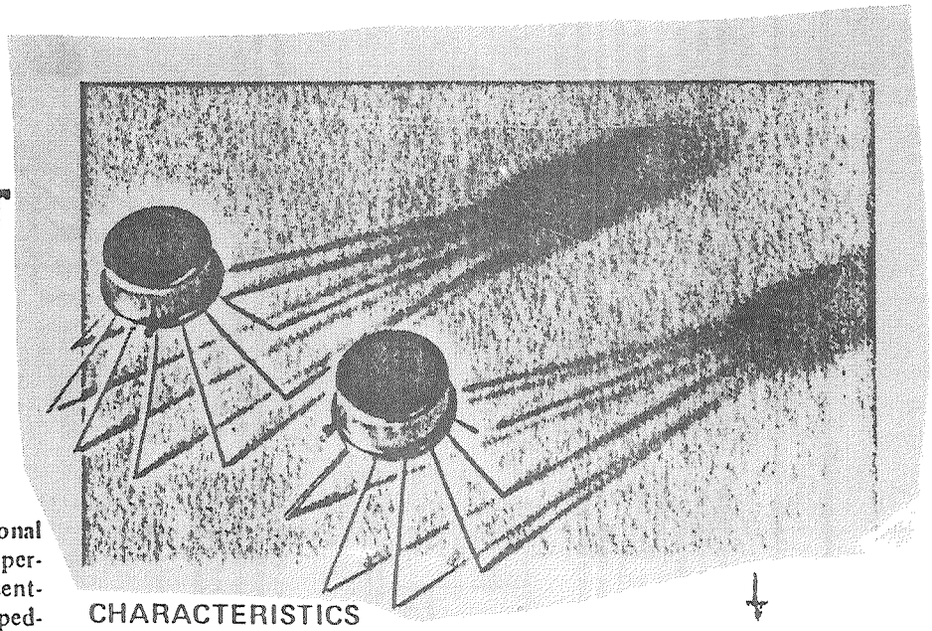
Free Running Operation

With the circuit connected as shown, it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle is set by the ratio of these two resistors, and the capacitor charges and discharges between $1/3V_{CC}$ and $2/3V_{CC}$. Charge and discharge times, and therefore frequency, are independent of supply voltage. The free running frequency versus R_A, R_B, and C is shown in the graph.





FA550/551 MONOLITHIC FET-DIFFERENTIAL-INPUT OPERATIONAL AMPLIFIERS



- $10^{12}\,\Omega$ Input Impedance
- 5pF Input Capacitance
- Unity-Gain Bandwidth to 10MHz
- Slew Rate to 120V/μsec
- 1pA Input Bias Current

The FA550 and FA551 Monolithic Operational Amplifiers are low-cost, subminiaturized, high-performance units with FET differential input, presenting a unique combination of ultra-high input impedance extremely low current offset and input capacitance, high slewing rate with equal response at either input terminal, and high common-mode rejection, with an output swing capability of ±10V at up to ±10mA. The two models offer trade-off selection of open-loop gain (15×10^3 or 15×10^4), input offset voltage (±30mV or ±15mV), bandwidth 8MHz or 10MHz unity-gain, 2MHz or 600kHz full-power, slew rate (120V/μsec or 35V/μsec) and settling time (400nsec or 2μsec, to 0.1%), at a slight price differential. They are packaged in standard TO-99 cases, with eight leads; unity-gain frequency compensation can be accomplished by connection of a single external capacitor, and input offset voltage is adjustable to zero by means of an external potentiometer connected to the trim terminals.

APPLICATIONS

- High-impedance, wideband comparators and amplifiers.
- High-speed integrators, sample and holds, peak detectors.
- Precision electrometer and photomultiplier amplifiers.
- Video summing. Fast, high amplitude, pedestal-pulse or radar-pulse summation.
- In multiplexers, as fast follower or inverter buffers.

DESIGN/APPLICATION FEATURES

Power: The FA550 and FA551 require a power source of ±14.7 to ±15.3VDC at 6mA (FA550) or 4mA (FA551) quiescent, unloaded, and 18mA or 16mA, respectively, at rated load and output. They are relatively insensitive to supply voltage fluctuations, having a sensitivity of only 5μV/%.

Trimming: Input offset voltage is adjustable to zero by an external 100kΩ potentiometer connected across the trim terminals, with the wiper connected to +15V.

Thermal Stability: Both models have an offset-voltage temperature coefficient of 50μV/°C.

CHARACTERISTICS

(typical @ +25°C and ±15VDC supply unless otherwise noted)	FA550	FA551
OPEN LOOP GAIN		
DC rated load, V/V	15×10^3	15×10^4
INPUT CHARACTERISTICS		
Input Voltage Range, min. rated specifications	±12V	±12V
Common Mode Voltage Range, min.	±10V	±10V
Common Mode Rejection, DC	90dB	90dB
Input Offset Voltage		
+25°C, adjustable to zero	±30mV	±15mV
vs. Temperature	50µV/°C	50µV/°C
vs. Supply Voltage	5µV/%	5µV/%
Input Bias Current		
+25°C	1pA	1pA
vs. Temperature	2 x/10°C	2 x/10°C
Input Impedance	$10^{12}\Omega$	$10^{12}\Omega$
Input Capacitance	5pF	5pF
OUTPUT CHARACTERISTICS		
Output Voltage, min.	±10V	±10V
Output Current	±10mA min.	±10mA max.
DYNAMIC CHARACTERISTICS		
Frequency Response		
Unity Gain, Small signal, 3dB**	8MHz	10MHz
Full Power Frequency,	2MHz	600kHz
Slewing Rate	120V/µsec	35V/µsec
Settling Time		
to 0.1%	400nsec	2µsec
POWER SUPPLY		
Voltage, rated, VDC	±14.7/±15.3	±14.7/±15.3
Current, no load, quiescent	6mA	4mA
Current, rated load and output	18mA	16mA
TEMPERATURE* **		
Operating, rated specifications	0°C to +75°C	0°C to +75°C
Storage	−55°C to +125°C	−55°C to +125°C
DIMEN. & PINOUTS (page 77)	Figure U	Figure U
Nominal weight	1 ounce	1 ounce

*Offset balance pot (100kΩ) connections: Arm 1, Wiper 7, Arm 5

**Compensating Capacitor Connections (Unity Gain): 8pF pin 8 to ground.

*** Available with extended operating temperature range: −55°C to +125°C (suffix "M"). Consult factory for prices and availability.

DATEL SYSTEMS, INC.

LOW COST, 12 BIT HYBRID ANALOG TO DIGITAL CONVERTERS

ADC-HX, ADC-HZ SERIES

FEATURES

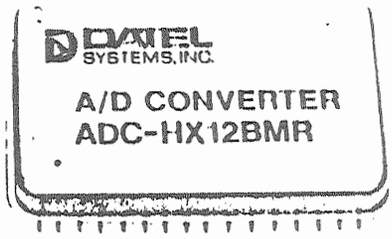
- 12 Bit Resolution
- 8 or 20μSec. Conversion
- Programmable Ranges
- Internal Buffer Amp.
- Short Cycle Capability
- Glass or Metal Package

GENERAL DESCRIPTION

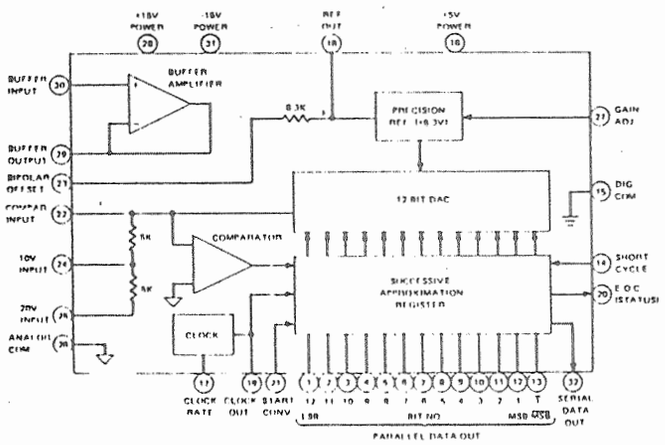
The ADC-HX12B and ADC HZ12B are self-contained, high performance, 12 bit A/D converters manufactured with thin-film hybrid technology. They use the successive approximation conversion technique to achieve a 12 bit conversion in 20 and 8 microseconds respectively. Five input voltage ranges are programmable by external pin connection: 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V. An internal buffer amplifier is also provided for applications where 100 megohm input impedance is required.

These converters utilize a fast 12 bit DAC consisting of tightly matched monolithic quad current switches, a stable nichrome thin-film resistor network, and a precision zener reference source. The circuit also contains a fast monolithic comparator, a monolithic 12 bit successive approximation register, a clock, and a monolithic buffer amplifier. The thin-film resistor network is functionally trimmed by a laser to precisely set the 8-4-2-1 current weighting in the quad current switches. The close tracking of the thin-film resistor and quad current switches result in a differential nonlinearity tempco of only ±2ppm/°C. Gain tempco is ±20ppm/°C maximum.

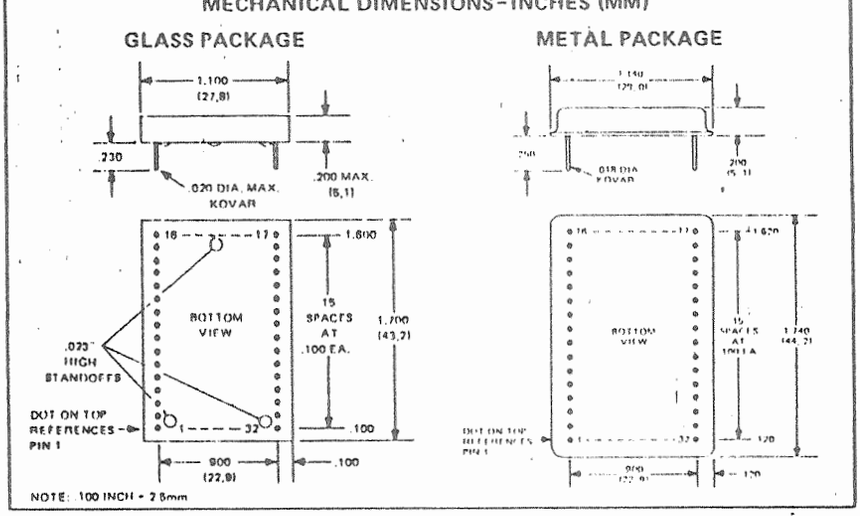
Both models have identical operation except for conversion speed. They can be short-cycled to give faster conversion in lower resolution applications. Use of the internal buffer amplifier increases conversion time by 3μsec., the settling time of the amplifier. Output coding is complementary binary, complementary offset binary, or complementary 2's complement. Serial data is also brought out. The package is a 32 pin hermetically sealed glass or metal case. Six different models are offered covering the operating temperature ranges of 0 to 70°C, -25 to +85°C, and -55 to +100°C.



(ACTUAL SIZE)



MECHANICAL DIMENSIONS - INCHES (MM)



SPECIFICATIONS
(Typical at 25°C, ±15V and +5V supplies unless otherwise noted)

	ADC-HX12B	ADC-HZ12B
INPUTS		
Analog Input Ranges, unipolar	0 to +5V, 0 to +10V FS	
Analog Input Ranges, bipolar	±2.5V, ±5V, ±10V FS	
Input Impedance	2.5K (0 to +5V, ±2.5V) 5K (0 to +10V, ±5V) 10K (±10V)	
Input Impedance with Buffer	100 Megohms	
Input Bias Current of Buffer	125nA typ., 250nA max.	
Input Overvoltage	±15V	
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 100nsec. min. Rise and fall times <30nsec. Logic "1" to "0" transition resets converter and initiates next conversion. Loading: 1 TTL load	
OUTPUTS[1]		
Parallel Output Data	12 parallel lines of data held until next conversion command. V_{OUT} ("0") < +0.4V V_{OUT} ("1") > +2.4V	
Coding, unipolar	Complementary Binary	
Coding, bipolar	Complementary Offset Binary Complementary Two's Complement	
Serial Output Data	NRZ successive decision pulses out, MSB first. Compl. Binary or Compl. Offset Binary Coding	
End of Conversion (Status)	Conversion status signal. Output is logic "1" during reset and conversion and logic "0" when conversion complete.	
Clock Output	Train of positive going +5V 100nsec. pulses, 600 kHz for ADC-HX12B and 1.5MHz for ADC-HZ12B (pin 17 grounded).	
PERFORMANCE		
Resolution	12 bits (1 part in 4096)	
Nonlinearity	±1/2 LSB max.	
Differential Nonlinearity	±1/2 LSB max.	
Gain Error, before adjustment	±0.1%	
Zero Error, unipolar, before adj.	±.05% of FSR[3]	
Offset Error, bipolar, before adj.	±0.1% of FSR[3]	
Temp. Coeff. of Gain	±20ppm/°C max.	
Temp. Coeff. of Zero, unipolar	±5ppm/°C of FSR max.[3]	
Temp. Coeff. of Offset, bipolar	±10ppm/°C of FSR max.[3]	
Diff. Nonlinearity Tempco	±2ppm/°C of FSR[3]	
No Missing Codes	Over oper. temp. range	
Conversion Time[2], 12 bits	20 µsec. max.	8.0 µsec. max.
10 bits[4]	15 µsec. max.	6.0 µsec. max.
8 bits[4]	10 µsec. max.	4.0 µsec. max.
Buffer Settling Time, 10V step	3.0 µsec. to .01%	
Power Supply Rejection	.002% / % Supply max.	
POWER REQUIREMENT		
	+15VDC ±0.5V @ 55mA −15VDC ±0.5V @ 45mA + 5VDC ±0.25 @ 100mA	
PHYSICAL-ENVIRONMENTAL		
Operating Temperature Range	0 to 70°C, −25 to +85°C, or −55 to +100°C	
Storage Temperature Range	−65°C to +150°C	
Package Size	1.70 X 1.10 X 0.2 inches (Glass) 1.74 X 1.14 X 0.2 inches (Metal)	
Package Type	Hermetically sealed glass or metal	
Pins	Kovar	
Weight	0.42 oz. (glass), 0.53 oz. (metal)	

NOTES:
1. All digital outputs can drive 2 TTL loads.
2. Without buffer amplifier used.
3. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input.
4. Short cycled operation.

TECHNICAL NOTES

1. It is recommended that the ±15V power input pins both be bypassed to ground with a .01µF ceramic capacitor in parallel with a 1µF electrolytic capacitor and the +5V power input pin be bypassed to ground with a 10µF electrolytic capacitor as shown in the connection diagrams. In addition, pin 27 should be bypassed to ground with a .01µF ceramic capacitor. These precautions will assure noise free operation of the converter.
2. Digital Common (pin 15) and Analog Common (pin 26) are not connected together internally, and therefore must be connected as directly as possible externally. It is recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 26 whereas digital ground and +5V ground should be run to pin 15.
3. External adjustment of zero or offset and gain are provided for by trimming potentiometers connected as shown in the connection diagrams. The potentiometer values can be between 10K and 100K ohms and should be 100ppm/°C cermet types (such as Datel Systems TP series). The adjustment range is ±0.2% of FSR for zero or offset and ±0.3% for gain. The trimming pots should be located as close as possible to the converter to avoid noise pickup. In some cases, for example 8 bit short-cycled operation, external adjustment may not be necessary.
4. Short cycled operation results in shorter conversion times where the conversion can be truncated to less than 12 bits. This is done by connecting pin 14 to the output bit following the last bit desired. For example for an 8 bit conversion, pin 14 is connected to bit 9 output. Maximum conversion times are given for short-cycled conversions of 8 or 10 bits. In these two cases the clock rate is also speeded up by connecting the clock rate adjust (pin 17) to +5V (10 bits) or +15V (8 bits). The clock rate should not be arbitrarily speeded up to exceed the maximum conversion rate at a given resolution, however, or missing codes will result.
5. Note that output coding is complementary coding. For unipolar operation it is complementary binary and for bipolar operation it is complementary offset binary or complementary 2's complement. In cases where bipolar coding of offset binary or 2's complement is required, this can be achieved by inverting the analog input to the converter (using an op amp connected for gain of −1.0000). The converter is then calibrated so that −FS analog input gives an output code of 0000 0000 0000, and +FS −1LSB gives 1111 1111 1111.
6. These converters dissipate approximately 2 watts of power. The case to ambient thermal resistance is approximately 25°C per watt. For ambient temperatures above 50°C, care should be taken not to restrict air circulation in the vicinity of the converter.

ORDERING INFORMATION

MODEL	TEMP. RANGE	CASE	PRICE (1-24)
ADC-HX12BGC	0 to 70C	GLASS	
ADC-HX12BMC	0 to 70C	METAL	
ADC-HX12BMR	-25 to +85C	METAL	
ADC-HX12BMM	-55 to +100C	METAL	
ADC-HZ12BGC	0 to 70C	GLASS	
ADC-HZ12BMC	0 to 70C	METAL	
ADC-HZ12BMR	-25 to +85C	METAL	
ADC-HZ12BMM	-55 to +100C	METAL	

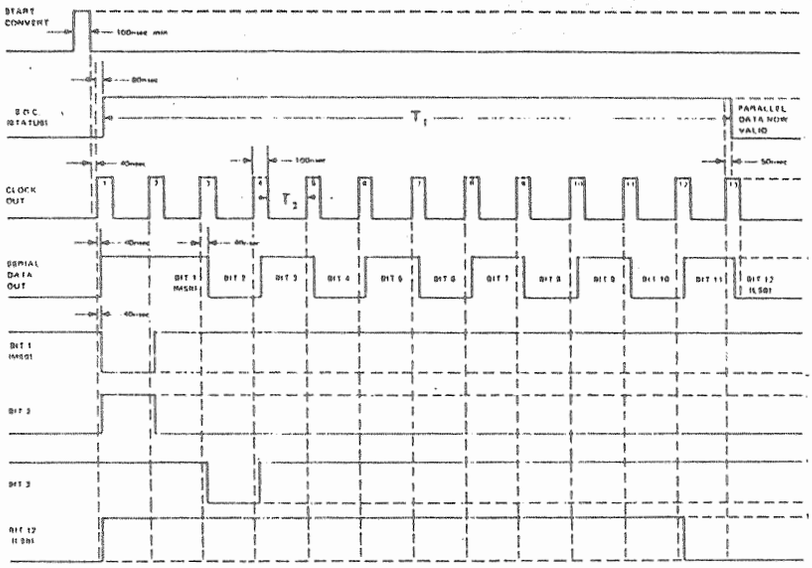
Mating Socket: DILS-2 (2/converter)

Trimming Potentiometers: TP2K, TP5K, TP10K, TP20K, TP50K or TP100K

THESE CONVERTERS ARE COVERED UNDER GSA CONTRACT

TIMING AND CONNECTION DIAGRAMS

TIMING DIAGRAM FOR ADC-HX12B, ADC-HZ12B OUTPUT: 010101010101

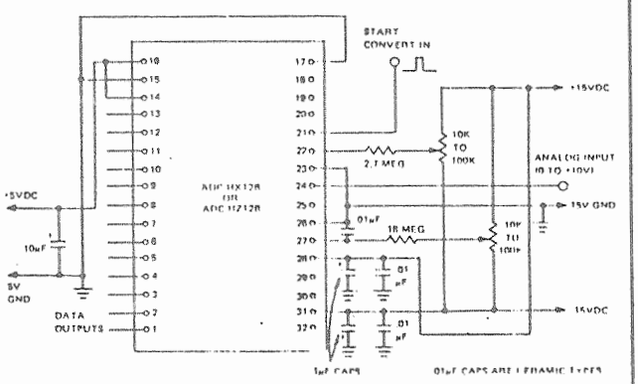


INPUT/OUTPUT CONNECTIONS

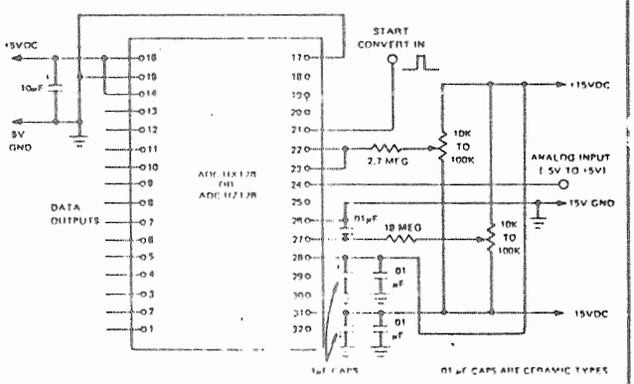
PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	17	CLOCK RATE
2	BIT 11 OUT	18	REF. OUT
3	BIT 10 OUT	19	CLOCK OUT
4	BIT 9 OUT	20	E.O.C. (STATUS)
5	BIT 8 OUT	21	START CONVERT
6	BIT 7 OUT	22	COMPAR. INPUT
7	BIT 6 OUT	23	BIPOLAR OFFSET
8	BIT 5 OUT	24	10V INPUT
9	BIT 4 OUT	25	20V INPUT
10	BIT 3 OUT	26	ANALOG COM
11	BIT 2 OUT	27	GAIN ADJUST
12	BIT 1 OUT (MSB)	28	+15V POWER
13	BIT 1 OUT ($\overline{\text{MSB}}$)	29	BUFFER OUTPUT
14	SHORT CYCLE	30	BUFFER INPUT
15	DIGITAL COM.	31	15V POWER
16	+5V POWER	32	SERIAL OUTPUT

	ADC-HX12B	ADC-HZ12B
T_1	20 μsec.	8.0 μsec.
T_2	1.56 μsec.	0.56 μsec.

UNIPOLAR OPERATION, 0 TO +10V



BIPOLAR OPERATION, -5V TO +5V



CODING TABLES

UNIPOLAR OPERATION

INPUT RANGE		COMP. BINARY CODING			
0 TO +10V	0 TO +5V	MSB			LSB
+9.9976V	+4.9988V	0000	0000	0000	
+8.7500	+4.3750	0001	1111	1111	
+7.5000	+3.7500	0011	1111	1111	
+5.0000	+2.5000	0111	1111	1111	
+2.5000	+1.2500	1011	1111	1111	
+1.2500	+0.6250	1101	1111	1111	
+0.0024	+0.0012	1111	1111	1110	
0.0000	0.0000	1111	1111	1111	

BIPOLAR OPERATION

INPUT VOLTAGE RANGE			COMP. OFFSET BINARY			COMP. TWO'S COMPLEMENT			
±10V	±5V	±2.5V	MSB		LSB	MSB			LSB
+9.9951V	+4.9976V	+2.4988V	0000	0000	0000	1000	0000	0000	
+7.5000	+3.7500	+1.8750	0001	1111	1111	1001	1111	1111	
+5.0000	+2.5000	+1.2500	0011	1111	1111	1011	1111	1111	
0.0000	0.0000	0.0000	0111	1111	1111	1111	1111	1111	
−5.0000	−2.5000	−1.2500	1011	1111	1111	0011	1111	1111	
−7.5000	−3.7500	−1.8750	1101	1111	1111	0101	1111	1111	
−9.9951	−4.9976	−2.4988	1111	1111	1110	0111	1111	1110	
−10.0000	−5.0000	−2.5000	1111	1111	1111	0111	1111	1111	

CONNECTIONS AND CALIBRATION

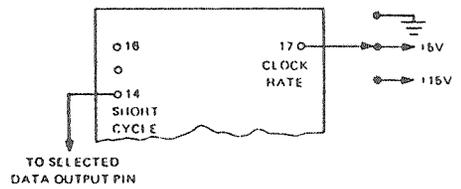
DATEL

INPUT CONNECTIONS

INPUT VOLT. RANGE	WITHOUT BUFFER			WITH BUFFER			
	INPUT PIN	CONNECT THESE PINS TOGETHER		INPUT PIN	CONNECT THESE PINS TOGETHER		
0 TO +5V	24	22 & 25	23 & 26	30	22 & 25	23 & 26	29 & 24
0 TO +10V	24	—	23 & 26	30	—	23 & 26	29 & 24
±2.5V	24	22 & 25	23 & 22	30	22 & 25	23 & 22	29 & 24
±5V	24	—	23 & 22	30	—	23 & 22	29 & 24
±10V	25	—	23 & 22	30	—	23 & 22	29 & 25

SHORT CYCLE OPERATION

CONNECTIONS



8, 10, & 12 BIT CONVERSION

RESOLUTION	12 BITS	10 BITS	8 BITS
ADC-HX12B CONV. TIME	20 µsec.	15 µsec.	10 µsec.
ADC-HZ12B CONV. TIME	8 µsec.	6 µsec.	4 µsec.
CONNECT THESE PINS TOGETHER	17 & 15 14 & 16	17 & 16 14 & 2	17 & 28 14 & 4

CLOCK RATE VS. VOLTAGE

PIN 17 VOLTAGE	CLOCK RATE	
	ADC-HX12B	ADC-HZ12B
0V	600 kHz	1.5MHz
+5V	720 kHz	1.8MHz
+15V	880 kHz	2.2MHz

PIN 14 CONNECTION

RES. (BITS)	PIN 14 TO
1	PIN 11
2	PIN 10
3	PIN 9
4	PIN 8
5	PIN 7
6	PIN 6

RES. (BITS)	PIN 14 TO
7	PIN 5
8	PIN 4
9	PIN 3
10	PIN 2
11	PIN 1
12	PIN 16

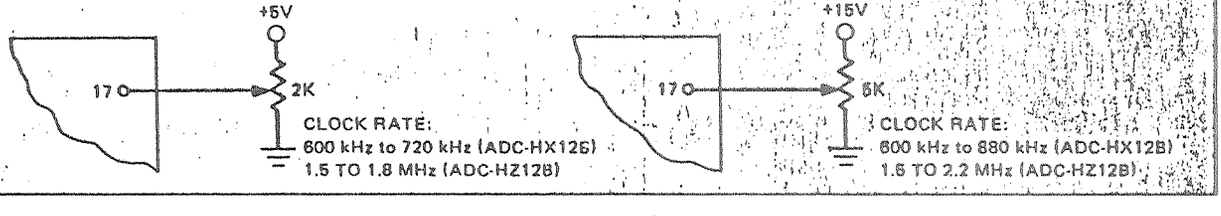
CALIBRATION PROCEDURE

1. Connect converter as shown in the Standard Connection diagrams. Use the Input Connection Table for the desired input voltage range and input impedance. Apply Start Convert pulses of 100 nsec. minimum duration to pin 21. The spacing of the pulses should be no less than the maximum conversion time.
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the selected analog input and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (zero +½ LSB) or the bipolar offset adjustment (FS+½ LSB). Adjust the trimming potentiometer so that the output code flickers equally between 1111 1111 1111 and 1111 1111 1110.
3. **Full Scale Adjustment**
   Change the output of the precision voltage reference source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS–1½ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 0000 0000 0001 and 0000 0000 0000.

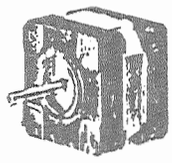
CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 TO +5V	ZERO	+0.6 mV
	GAIN	+4.9982V
0 TO +10V	ZERO	+1.2 mV
	GAIN	+9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET	–2.4994V
	GAIN	+2.4982V
±5V	OFFSET	–4.9988V
	GAIN	+4.9963V
±10V	OFFSET	–9.9976V
	GAIN	+9.9927V

EXTERNAL CLOCK RATE ADJUSTMENT

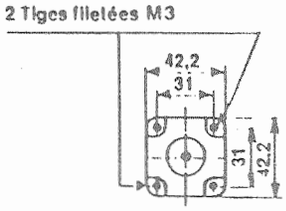


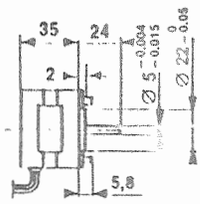
Présentation



Encombrement

2 Tiges filetées M3



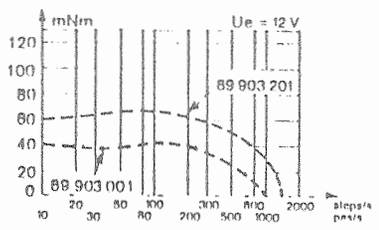


	symbole	unité	89 903 201	89 903 001
Angle de pas	α	°	1,8°	
Nombre de phases	m		2	4
Tension moteur	Um	V	9	12
Résistance par phase	R	Ω	38	75
Inductance par phase	L	mH	45	45
Intensité par phase	I	A	0,24	0,16
P. absorbée par le moteur	Pa	W	4,3	3,8
Couple de maintien	Mh	mN.m	60	50
Couple de détente	Ms	mN.m	6	
T. maxi bobinage		°C	105	
T. ambiante	Tam	°C	− 10 à + 50	
T. stockage	Ts	°C	− 40 à + 105	
Inertie du rotor	Jr	g.cm²	15	
Tension d'isolement (50 Hz)		V	600	
Masse du moteur	M	g	260	
Commande électronique				89 990 001
Constante de temps	τ	s		

Courbe N° 1

Courbes limites en arrêt-démarrage ——

Courbes limites d'entrainement - - - - - - -



Fréquence limite d'entrainement en fonction de l'inertie

Schéma des connexions du moteur